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The Combined Effects of Radio Frequency and Gamma Irradiation on P-Channel MOSFETs

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THESIS

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Abstract

The purpose of this research was to investigate the combined effects of continuous gigahertz radio frequency signals and gamma irradiation on the threshold voltage of metal oxide semiconductor field effect transistors. The combined effects of gigahertz radio frequency waves and gamma irradiation on electronics presents a new challenge in electronic warfare and little is known of the combined effect on threshold voltage damage and recovery. The Fairchild NDS352AP, a commonly used commercial device, was irradiated by a cobalt-60 source under a +5 V bias with and without a radio frequency signal applied to the gate. The threshold voltage was measured during and after irradiation. During irradiation all devices exhibited an expected negative threshold voltage shift. The application of radio frequency to the gate resulted in a 7.2% increase in the rate of change of the threshold voltage during irradiation. When RF was applied after irradiation it produced no observable change when compared to the results of samples exposed to gamma radiation alone. Few conclusions can be drawn about the effects of radio frequency on the samples following irradiation owing to the long recovery time of the samples. Before irradiation the radio frequency produced a 5.95% increase in drain current for a given drain to source voltage during I-V measurements. The threshold voltage also increased by 1.57%. The power of the radio frequency signal was adjusted from 1 to 14 dBm with no measurable effect.

Table of Contents

List of Figures

List of Tables

Table Page

THE COMBINED EFFECTS OF RADIO FREQUENCY AND GAMMA IRRADIATION ON P-CHANNEL MOSFETS

I. Introduction

1.1 Overview

The threat of weapons which disable electronic devices is growing rapidly as our societal infrastructure becomes more reliant upon electronics. A direct attack on these systems could be devastating, affecting our defensive systems, telecommunications, and personal electronics. High power microwave (HPM) weapons provide an increasing threat in modern electronic warfare. With portable HPM systems able to affect targets at ranges up to 500 m [11], the Air Force and the Department of Defense have a profound interest in preventing damage and hardening systems against high power microwave effects.

The metal oxide semiconductor field effect transistor (MOSFET) is a common component in many electronic devices including cellular telephones, communication systems, and computers. A disruption in an integrated MOSFET circuit within these devices may cause temporary or even permanent damage. HPM systems are currently known to be able to drive large amounts of current which will permanently disable electronic components [11]. Ionizing radiation can also cause device damage and can effect proper device operation. An HPM attack combined with ionizing radiation has the

potential to disrupt the device or damage it beyond its operational limits. The purpose of this research is to investigate the effects of a gigahertz radio frequency (RF) signal applied to the gate of MOSFETs during and after irradiation with an ionizing radiation source. Applying a RF wave to the gate will act to simulate a free field HPM attack, representing the power coupled to the gate of the MOSFET.

1.2 Hypothesis

Radiation damage on MOSFETs is a well documented phenomenon. RF effects are less documented but some data is available [11][20][21]. The combined effects are not well documented and the outcome was unclear at the beginning of this research. The RF signal applied to the gate will also have an effect on the MOSFET, particularly the threshold voltage characteristics, potentially by interacting with holes in the oxide and lengthening their time in the oxide. This would lead to more hole trapping or decrease the rate of hole transport and recombination. The threshold voltage is expected to decrease and the recovery time to increase with a RF signal applied to the gate. The transfer and output characteristics will also be changed by the introduction of a RF signal on the gate. This is expected because the RF may cause the holes to oscillate within the oxide which increases the chance of trapping. Without a RF signal applied to the gate, gamma radiation will cause the threshold voltage to shift negative for a p-channel device.

Adding a positive gate bias during irradiation is expected to increase the rate of negative threshold voltage shift due to the field sweeping electrons from the oxide even more rapidly. The less time each electron spends within the oxide layer, the less chance it has for recombination. Therefore, less recombination will occur within the oxide with

a bias applied during irradiation resulting in more holes within the oxide and a lower threshold voltage. Applied gate bias during recovery is expected to accelerate the rate of recovery due to the electric field pushing oxide holes to the interface where they can tunnel out of the oxide. The addition of a RF signal to the gate is expected to increase the rate of negative threshold voltage shifting and slow or even halt device recovery.

1.3 Thesis Structure

This document begins by presenting the fundamental theory behind the MOSFET and its response to external influences such as ionizing radiation and RF signals. A historical overview, theory behind the device structure and operation, current-voltage and capacitance-voltage relationships for the gate capacitor, ionizing radiation effects, and the effects RF are contained in Chapter 2. Chapter 3 outlines the experimental procedures used to characterize the device. Chapter 4 discusses the results of the data from the experimental testing. Chapter 5 adds suggestions for future research.

II. Theory

2.1 Overview

The MOSFET is an electronic device used as a low power gain switch and can be used to amplify current in an electronic circuit. MOSFETs are used for very low current circuits and are particularly important for integrated circuit technology where power limitations are a major consideration. They are commonly used for integrated circuits owing to their low power consumption, greatly reduced heat generation, and the high yield of working devices using modern fabrication techniques. The MOSFET is a technological benchmark and is the most widely used transistor in existence, providing the cornerstone of nearly all integrated electronics to date [23].

A silicon MOSFET was chosen for this research because silicon is one of the most common elements used to fabricate electronics. It is one of the most common materials used in MOSFETs owing to a relatively simple and low cost production method and because it forms a very good semiconductor-to-insulator interface with SiO_2. Thermally grown Si/SiO_2 interface technology has developed greatly over several decades to be of high quality, having a lower defect density, and resulting in a very abrupt junction at the interface.

Standard silicon MOSFETs can be classified as one of two types depending on the doping in the channel region. A p-channel field effect transistor (PFET) has a channel region that conducts holes when turned on with a substrate that is doped n-type. An n-channel field effect transistor (NFET) has a channel region that concuts electrons when turned on with a substrate that is doped p-type. N-channel silicon MOSFETs tend

to be more prominent in radiation testing owing to p-type silicon having more vulnerability to ionizing radiation. For the purpose of this research a p-channel MOSFET was chosen because it is one of the essential components of metal oxide semiconductor (MOS) memory and is less sensitive to ionizing radiation than the n-channel MOSFET. It was expected that high sensitivity to dominant ionizing radiation effects may have lead to the lack of substantial RF results in this research.

2.2 Historical Overview

The MOSFET was first proposed in 1925 by Dr. Julius E. Lilienfield [27]. However, its potential was not fully realized until the mid 1960's. This delay was due to problems with growth and processing particularly in interfacing with oxide layers. The first MOS transistor was built in 1960 at Bell Laboratories. Kahng and Atalla, are credited with the discovery of the MOSFET in 1960 [23]. During the mid 1960's the MOSFET and MOS integrated circuits were further demonstrated. The MOSFET replaced the Bipolar Junction Transistor (BJT) (invented in 1945 at Bell Laboratories) in most electronic applications by the 1980's [23]. The usefulness of the MOSFET in integrated circuit technology was a primary reason for the boom of the now multi-billion dollar semiconductor device industry [27]. MOSFET technology has laid the groundwork and served as a catalyst for microelectronic use and integrated circuit technology to date.

2.3 Device Specifics of a P-Channel MOSFET

A typical p-channel MOSFET has the structure shown in Figure 1.

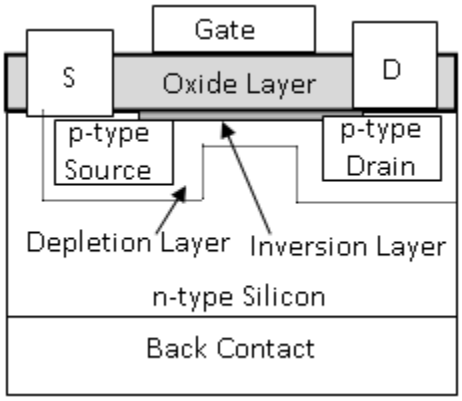


Figure 1. Cross sectional view of the p-channel MOSFET

The device chosen for this thesis is the Fairchild NDS352AP enhancement mode p-channel MOSFET. P-channel defines the primary carriers in the channel region as holes, which means that holes are the majority carrier which flow through the channel when the transistor is in conduction mode. The channel region is defined as the area under the gate which connects the source and the drain. The device chosen is also an enhancement mode device. Enhancement mode means that it is normally in the off state. The MOSFET has a negligible source to drain current when no voltage is applied to the gate. When a negative gate voltage is applied to a p-channel MOSFET the majority carriers (electrons) will be depleted in the channel. When the magnitude of the field from the gate voltage is sufficient the minority carriers (holes) form a conduction channel at the Si/SiO_2 interface. This conduction channel allows current to flow between the source and drain regions. This behavior is demonstrated in Figure 2.

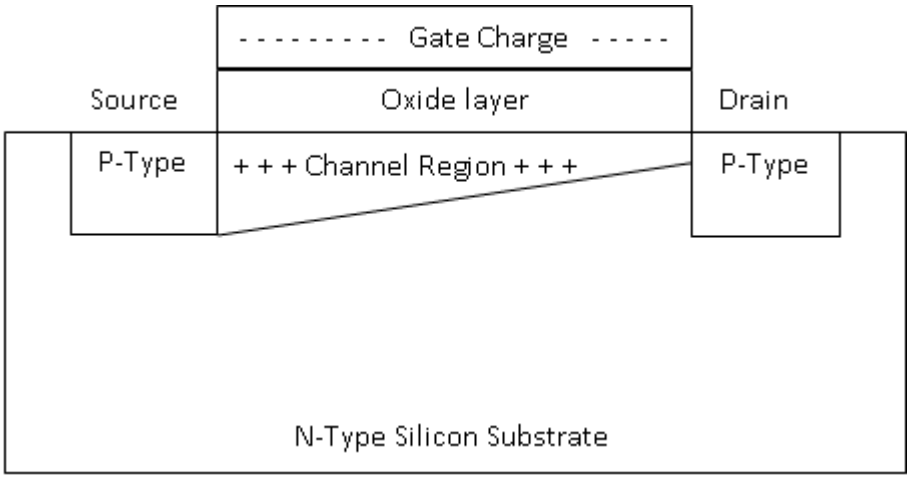


Figure 2. Behavior of p-channel region in an enhancement mode MOSFET

At this point the channel is considered to be on. The minimum voltage needed to turn on the device is known as the threshold voltage and will be more thoroughly examined in section 2.7.

2.4 I-V Characteristics

In the case of the MOSFET the output and transfer characteristics are key design and performance parameters. The output characteristics are illustrated by plotting the drain-to-source current against the drain-to-source voltage. An example curve, with varying gate bias, is shown in Figure 3.

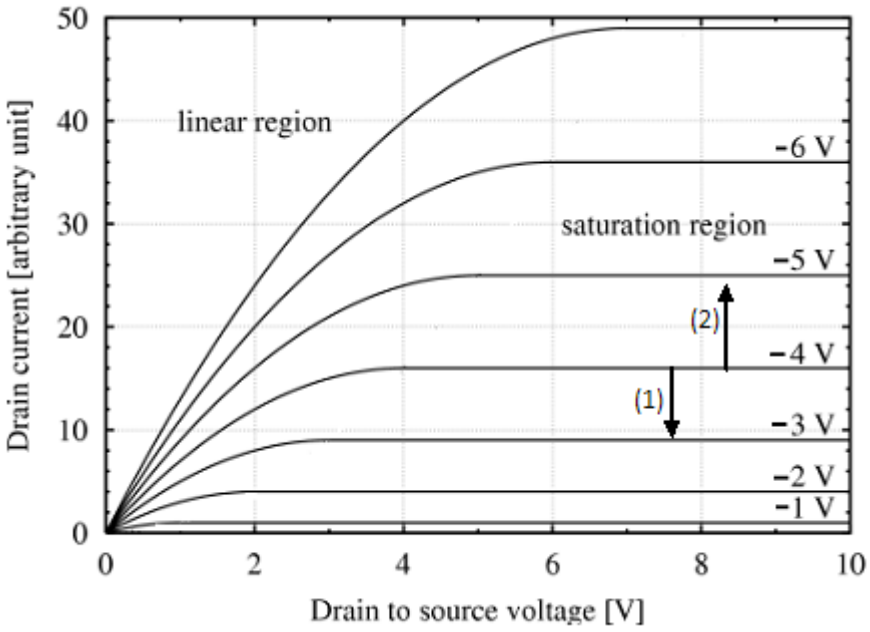


Figure 3. Example MOSFET I-V output characteristics [23]

For a p-channel MOSFET, the I-V characteristics can change as shown in Figure 3. By changing the gate voltage the curves will shift but the threshold voltage of the device will not change. Ionizing radiation or a RF signal can cause the I-V curve at a given gate voltage to shift, resulting in changes in threshold voltage. The downward shift labeled (1) occurs due to decreasing the magnitude of the gate voltage or an increase in trapped oxide holes (discussed in detail later). The downward shift in the drain current relates to a negative threshold voltage change and is referred to as a negative shift in the I-V curve. Similarly increasing the magnitude of the gate voltage or fewer trapped oxide holes will cause an upward shift, labeled as (2), and an increase in threshold voltage. The behavior labeled in (2) is considered a positive I-V shift for p-channel devices. In the case of p-channel and n-channel MOSFETs a primary difference is the sign of the voltage applied to the gate to turn on the devices. Other differences include cost, mobility,

timing, and functionality. The primary cause for differences in timing and functionality relates to the mobility of the primary carrier within the channel. Electrons have a mobility of 20 $cm^2V^{-1}s^{-1}$ within SiO_2 at room temperature [15]. The mobility of holes is temperature and field dependent but is always orders of magnitude lower than electrons, ranging from 10^{-4} to 10^{-11} $cm^2V^{-1}s^{-1}$ in SiO_2 [15]. When measuring p-channel MOSFETs the interest is the voltage between the gate and source.

The transfer characteristics are illustrated by plotting the drain-to-source current against the gate-to-source voltage. A graph that illustrates the transfer characteristics of a MOSFET is shown in Figure 4.

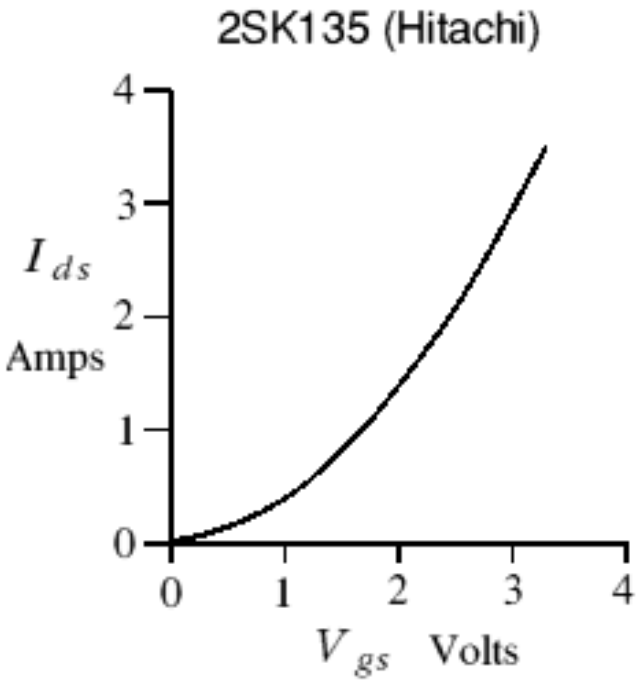


Figure 4. Example I-V transfer characteristics of a p-channel MOSFET [7]

2.5 Capacitance-Voltage Characteristics

During the Capacitance-Voltage (C-V) measurement the voltage on the gate is increased causing the MOSFET to transition from accumulation to inversion while constantly measuring the capacitance. Accumulation and inversion will be explained further in sections 2.8.1 and 2.8.3 respectively. As shown in Figure 1, the MOS structure forms a permanent capacitor through the oxide layer. This layer contributes to an oxide capacitance within the circuit. When a negative gate voltage is applied, the electrons within the silicon move away from the channel region. This creates a second, variable capacitor out of the space charge left behind. The space charge capacitance is in series with the oxide capacitor. The C-V measurement provides a response to the combined oxide and semiconductor capacitances in series and can be used to determine threshold voltage or the quality of the interface. A simulated C-V measurement illustrating the capacitance as a function of applied voltage for a p-channel MOSFET is shown in Figure 5.

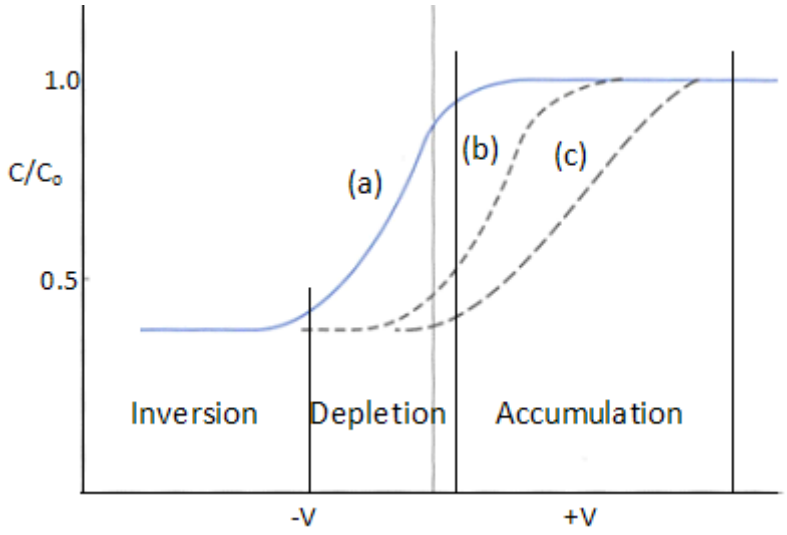


Figure 5. C-V measurement of a p-channel MOSFET modeled as (a) ideal (b) common production impurities (c) radiation damaged or poorly manufactured [23]

The regions are marked for the curve labeled (a). The following assumptions are used to model the curves shown in Figure 5 [23]. Curve (a) assumes an ideal MOSFET. Curve (b) includes the flat band voltage shift that originates from nonzero work function difference (φ_{ms}), fixed charge (Q_f), oxide trapped charges (Q_{ot}), or mobile ionic charges (Q_m). These impurities are often introduced in the production of the MOSFET. Curve (c) illustrates the addition of very large amounts of oxide trapped charges which vary with surface potential and additional interface traps within the semiconductor, resulting in a change of shape. The distortion of the shape is due to the interface trapped charges while the parallel shift of the curve is due to the oxide trapped charges [23]. Radiation damage commonly increases the number of oxide trapped holes. These trapped oxide charges will displace the C-V curve even further as shown in Figure 5 condition (c).

2.6 Flat Band Voltage

While the Si/SiO_2 interface is widely used and is nearly ideal, the commonly used metal electrodes can affect MOS characteristics. The work function is the energy difference between the vacuum level and the Fermi level and it varies with doping concentration [23]. For Si/SiO_2 the work function difference is typically non-zero. Work function differences cause band bending downward while in equilibrium. In order to achieve an ideal flat band condition a voltage must be applied which is equal to the work function difference. An energy band diagram of the flat band condition is shown in Figure 6.

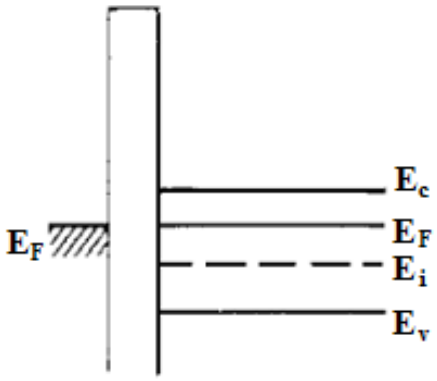


Figure 6. Energy band diagram for a p-channel MOSFET in flat band condition [15]

Figure 6 uses the following abbreviations: E_c is the conduction band energy level, E_F is the Fermi level, E_i is the intrinsic energy level and E_v is the valence band energy level. This same notation will follow in all figures containing energy band diagrams. This applied voltage is called the flat band voltage and is given by equation (1). Equations used throughout this chapter were developed using chapter 5 of Sze as a model [23].

$$V_{FB} = q\left(\phi_m - \phi_s\right) \tag{1}$$

In equation (1), $q\varphi_m$ is the work function of the metal and $q\varphi_s$ is the work function of the substrate. The work function has units of volts. For metal-Si-SiO_2 the flat band voltage is not expected to be over 2V, depending on the electrode materials and silicon doping concentration. For a non-equilibrium state or an arbitrary space charge distribution within the oxide, a general equation for flat band voltage is given as:

$$V_{FB} = \frac{-1}{C_o}\left[\frac{1}{d}\int_0^d x\rho(x)\,dx\right]. \tag{2}$$

In equation (2) C_o is the oxide capacitance per unit area, d is the thickness of the oxide, x is the location within the oxide, and $\rho(x)$ is the volume charge density within the oxide.

Aside from the materials used in the device there are three other factors that influence the flat band voltage. These factors include fixed oxide charge, oxide trapped charge and mobile ionic charge. The fixed charge, denoted by Q_f, is located within 3 nm of the Si-SiO_2 interface [23]. The fixed charge is dependent on the oxidation conditions, annealing conditions, and silicon orientation. The oxide trapped charges, Q_{ot}, are directly related to the defects in the silicon dioxide. The mobile ionic charges, Q_m, are dependent on electric field and temperature conditions. Under high bias or high temperature conditions the mobile ionic charges move throughout the oxide layer and cause shifts in the C-V characteristics. The fabrication process reduces mobile ionic charges; hence, their effect on flat band voltage and C-V characteristics is greatly reduced.

When the value of the work function difference is non-zero and the interface-trapped charges are negligible, then the C-V characteristic curves will be shifted from the theoretical amount, given by equation (1), by the flat band voltage given in equation (3).

$$V_{FB} = \phi_{ms} - \frac{\left(Q_f + Q_m + Q_{ot}\right)}{C_o} \tag{3}$$

2.7 Threshold Voltage

Threshold voltage is defined as the gate voltage at which an inversion layer forms at the interface between the insulating oxide and the substrate. This occurs when there are enough holes within the inversion layer to create a low resistance, conductive path from source to drain (through the channel region). The threshold voltage is calculated from the following:

$$V_T = \frac{\sqrt{2\varepsilon_s q N_A \left(2\psi_B\right)}}{C_o} + 2\psi_B \,. \tag{4}$$

In equation (4), q is the charge of an electron, N_A is the acceptor concentration, C_o is the oxide capacitance, and ψ_B is the potential required to bend the energy bands down to the intrinsic condition at the surface. The permittivity of silicon, ε_s, is given by:

$$\varepsilon_s = \varepsilon_r \varepsilon_o \,. \tag{5}$$

In equation (5), ε_r is the permittivity associated with silicon and ε_o is the permittivity of free space. For silicon ε_s is 1.05×10^{-12} $m^{-3}kg^{-1}s^4A^2$ and ε_r is 11.7 [13]. Equation (6)

contains an approximation for the surface potential, ψ_s, near inversion. It is assumed that near inversion the electron concentration at the surface is equal to the substrate impurity concentration, N_A. This yields the following:

$$\psi_s(inv) \approx 2\psi_B = \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right). \tag{6}$$

In equation (6), k is the Boltzmann constant, T is the temperature, and n_i is the intrinsic concentration. For silicon the intrinsic concentration is 9.86×10^9 cm^{-3} [13]. When not near inversion the surface potential is given as:

$$\psi_s = \frac{qN_A W^2}{2\varepsilon_s}. \tag{7}$$

In equation (7), W is the width of the surface depletion region given by:

$$W = \frac{qN_A}{Q_{gate}}. \tag{8}$$

In equation (8), Q_{gate} is the total charge placed on the gate. Charge neutrality governs the depletion width forcing the width to adjust in order to always balance the gate charge. A maximum width will eventually be reached and is described by:

$$W_m = 2\sqrt{\frac{\varepsilon_s kT\ln\left(\frac{N_A}{n_i}\right)}{q^2 N_A}}. \tag{9}$$

Precise control of the threshold voltage of MOSFETs in an integrated circuit is essential for reliable circuit operation [23]. Therefore, changes to the threshold voltage are of key importance to this research and will be a primary characteristic that is monitored and analyzed.

2.8 Modes of Operation

Assuming no residual charge in the oxide, once voltage is applied to the gate, the flat band condition no longer applies and the MOSFET can operate in one of three modes (depending on the magnitude and sign of the voltage applied to the gate). These modes are accumulation, depletion, and strong inversion. Each mode will cause a unique device response. These are outlined and discussed in the following subsections.

2.8.1 Accumulation Mode

While the gate voltage is positive and decreasing in magnitude to zero, the MOSFET is in accumulation mode. While in this mode the electric field from the voltage applied at the gate attracts electrons to the Si/SiO_2 interface. The electrons are at a greater concentration at the Si/SiO_2 interface than in the n-type silicon substrate bulk. This accumulation terminates the field lines at the gate and produces a dielectric thickness approximately equal to the thickness of the oxide layer. This condition produces the maximum capacitance within the device and is equal to the capacitance of the oxide layer. The band diagram of the MOS diode while in accumulation mode is illustrated in Figure 7. While in accumulation mode the majority carriers, electrons, still maintain a greater concentration at the Si/SiO_2 interface than the holes.

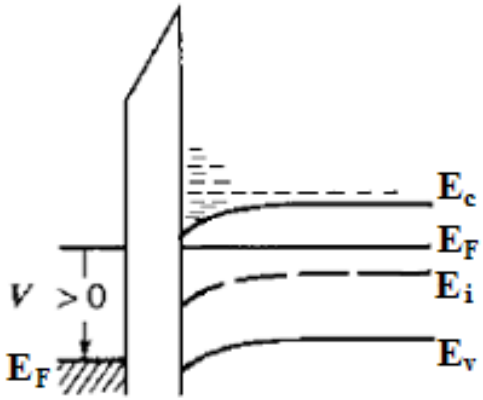


Figure 7. Energy band diagram for a p-channel MOSFET in accumulation mode [15]

2.8.2 Depletion Mode

As the gate voltage become negative and begins to approach the threshold voltage the MOSFET is considered to be in depletion mode. This occurs because the majority carriers, electrons, begin to repel away from the interface and diffuse throughout the bulk. This lack of electrons leaves an area of depleted carriers. While in this mode the negative electric field from the voltage applied at the gate begins to attract the holes to the Si/SiO_2 interface. The holes begin to accumulate in significant numbers at the silicon and oxide interface. The charge of the holes within the depleted layer will counter the applied gate voltage until the threshold voltage is reached. As the depletion layer expands the effective dielectric length increases which causes a decreasing capacitance as the voltage is increased. The capacitance of the channel region will add to the capacitance of the oxide layer in series as shown in equation (10).

$$\frac{1}{C_{ox}} + \frac{1}{C_{chan}} = \frac{1}{C_{tot}} \tag{10}$$

In equation (10), C_{ox} is the oxide capacitance, C_{chan} is the capacitance of the channel, and C_{tot} represents the total measured capacitance of the MOSFET. The energy band diagram for a p-channel device in depletion mode is shown in Figure 8.

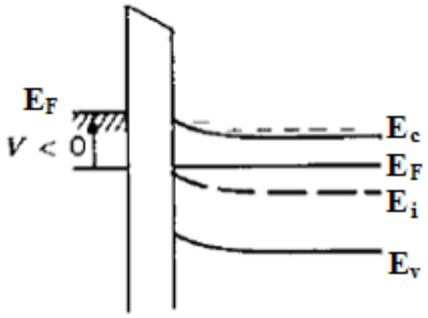


Figure 8. Energy band diagram for a p-channel MOSFET in depletion mode [15]

2.8.3 Strong Inversion Mode

Once the threshold voltage is reached and the gate voltage is further increased the MOSET enters strong inversion mode. Once in strong inversion all charge within the MOSFET is assumed to be within the inversion layer and the depletion region. The voltage at which strong inversion occurs is equivalent to the threshold voltage for a MOSFET. Strong inversion occurs when the concentration of holes near the interface is equal to the substrate doping level. The silicon surface begins behaving as if it is p-type owing to the high hole concentration. Once inversion is reached the depletion width and

the effective dielectric length can no longer increase. The depletion width is at its maximum value. This is because the bands are bent downward far enough that a small increase in band bending will result in a small increase in depletion layer width which results in a large increase in charge within the inversion layer. This rapid increase in inversion layer charge with gate voltage shields the interior of the semiconductor from any additional charge (or electric field) placed on the gate. The energy band diagram for a p-channel device in strong inversion is illustrated in Figure 9.

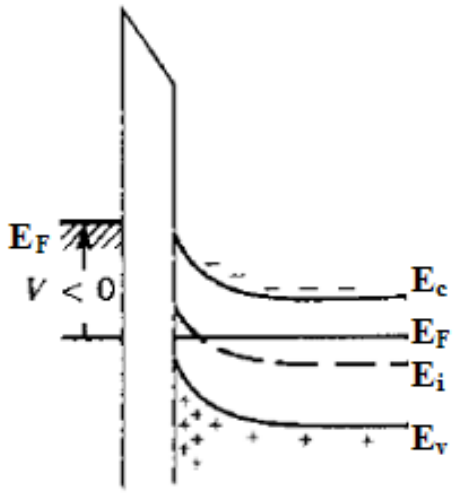


Figure 9. Energy band diagram for a p-channel MOSFET in strong inversion mode [15]

The maximum depletion width for silicon while in strong inversion mode is shown in Figure 10.

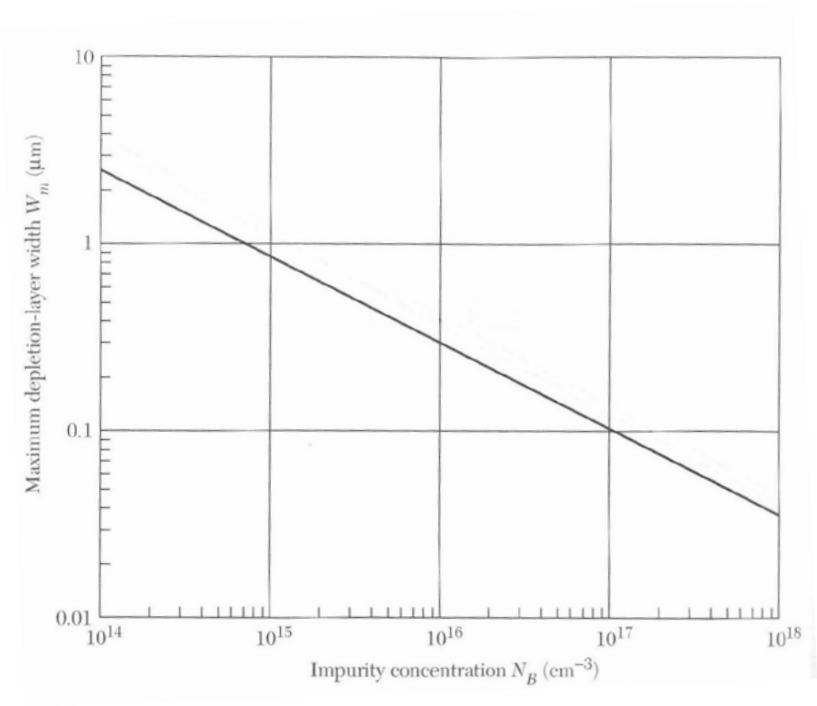


Figure 10. Maximum depletion layer width for silicon in strong inversion [23]

Once the depletion layer width reaches its maximum value, the total capacitance per unit area remains at a minimum value which effectively remains constant as described in Equation (11).

$$C_{\min} = \frac{\varepsilon_{ox}}{d + \left(\frac{\varepsilon_{ox}}{\varepsilon_s}\right) W_m} \tag{11}$$

In equation (11) ε_{ox} is the permittivity of the oxide layer and d is the width of the oxide layer. ε_s and W_m are described in equations (5) and (9) respectively.

2.9 Radiation Effects on MOSFET Devices

When modern electronics are exposed to ionizing radiation, holes are created within the substrate and oxide and lead to changes in device performance. Many modern MOSFETs, especially ones used for space based applications, operate in harsh radiation environments. Therefore, it is important to understand these effects and the damage that they can cause within a device. For this research a Co-60 source was chosen for irradiation due to its emission of relatively high energy gamma rays. Gamma rays are defined as quanta of electromagnetic energy with wavelengths between 10^{-13} and 10^{-11} m emitted from the decay of the nucleus [17]. When an atom undergoes radioactive decay an excited daughter nucleus is sometimes produced. This daughter nucleus de-excites to a lower energy state releasing energy in the form of gamma radiation. Co-60 beta decays (β-) to stable Ni-60 and releases two gammas with energy 1.17 and 1.33 MeV [13].

When exposed to ionizing radiation electrons and holes are created by electron-hole pair production. The electrons quickly move out of the oxide region but the holes are persistent and will remained trapped within the oxide layer even after the MOSFET is removed from the radiation source [15]. This will directly affect the Q_{ot} term in equation (3). This increase causes a negative flat band and threshold voltage shift [10]. Charges within the oxide, rather than on the oxide surface are responsible for most of the device total ionizing dose degradation [10]. Threshold voltage shifts are assumed to be caused by trapped charge in the gate oxide. This assumption is made owing to the oxide charges influencing threshold voltage much more than negative charge trapping or interface trap buildup [15]. The shift labeled (1) in Figure 3 demonstrates the expected shift in I-V

characteristics after exposure to gamma radiation. With more holes in the oxide, the negative electric field required to reach strong inversion (and threshold) increases. This means that the magnitude of the (negative) bias applied to the gate must be greater in order to obtain pre-irradiation drain current levels through the channel.

As total dose increases the trapped charges begin to saturate the device. High dose rates, typically higher than 10^6 rad/s, can induce currents high enough to interfere with proper device operation [15]. In this study, rates of irradiation remain below 100 rad/s so total dose as a function of time irradiated will be emphasized. As total dose increases a saturation dose can be reached. The saturation dose in SiO_2 is found to be 10^8-10^9 rad(Si) [6]. However, interface trapped charge may saturate at a higher total dose than oxide trapped charge. Interface trapped charge has been observed to saturate at doses between 10^{10} and 10^{12} rad(Si) [9]. In order to avoid SiO_2 saturation total dose in this study did not exceed 10^6 rad(Si).

The radiation induced trapped oxide charge decreases more rapidly with oxide thickness than interface trapped charge. The radiation induced interface trapped charge remains a major factor in limiting integrated circuit performance in modern integrated circuits. This is associated with reduced circuit speed owing to high radiation doses at low dose rates. Therefore, newer technology with thinner oxide layers, may begin to experience higher rates of device failure, in similar radiation environments, when compared to devices with thicker oxide layers.

2.10 RF Effects on MOSFET Devices

Gigahertz RF interference on modern devices can cause severe upsets in device operation [21]. A continuous wave (CW) gigahertz frequency source applied to a MOSFET circuit can cause significant changes in output current, transconductance, output conductance, and breakdown voltage [11]. Kim et al. suggest that sensitivity to RF effects is greatly diminished beyond the 5 GHz range [11]. Therefore, the RF applied to devices in this study was below 5 GHz. Kim also suggests that the primary changes induced will be present in the I-V output characteristics. Changes such as saturation and linearity in the amplification region or failure to turn on are likely to occur. Previous studies have demonstrated the changes in I-V output characteristics which are shown in Figure 11 and Figure 12.

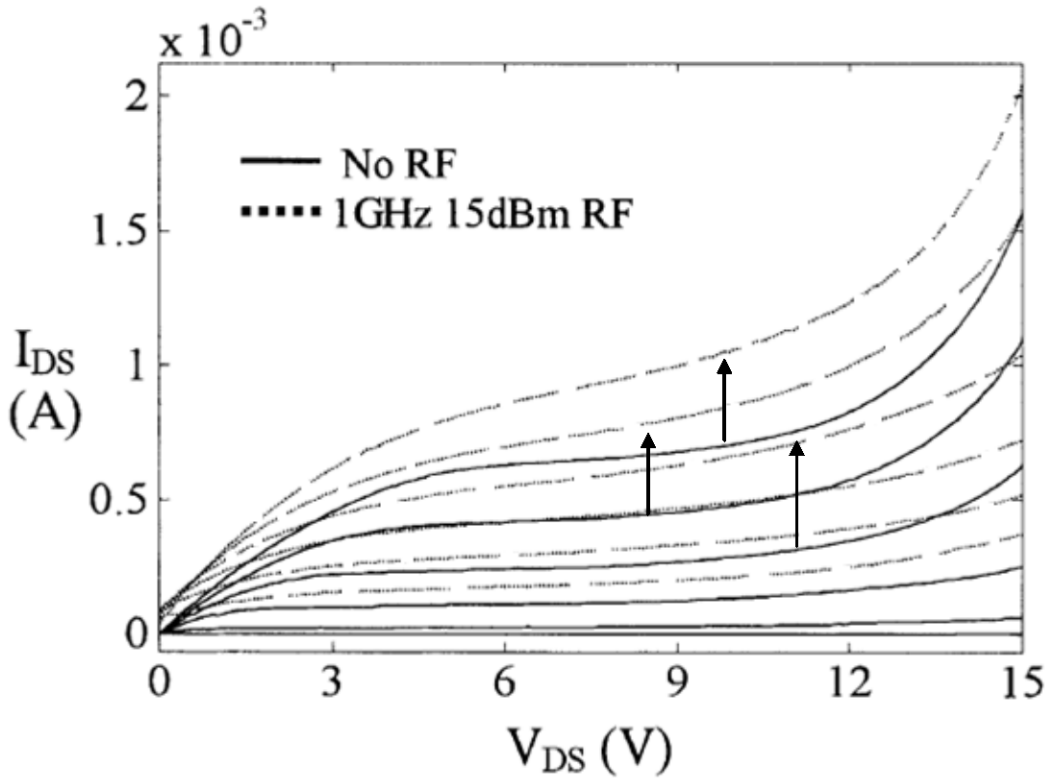


Figure 11. 15 dBm RF effects on I-V output characteristics of an n-channel MOSFET [11]

The 15 dBm RF signal applied to the gate causes the I-V curves to shift in the positive direction as shown in Figure 11. The shift for an n-channel is the inverse of a p-channel MOSFET. A positive shift means a lower threshold voltage for n-channel MOSFETs. The RF signal is interacting with the holes within the oxide and de-trapping them. The de-trapped holes move toward the channel region and either become trapped, recombine, or exit the oxide. More holes within the oxide explain the positive increase in the I-V curve. Therefore, the RF is increasing the number of trapped holes owing to oscillation within the oxide layer and an increased trapping probability. The saturation region has a positive slope owing to the hot electron effect. The RF is acting to add

energy to the electrons in the conduction band and changing their conduction mechanism through the channel [15].

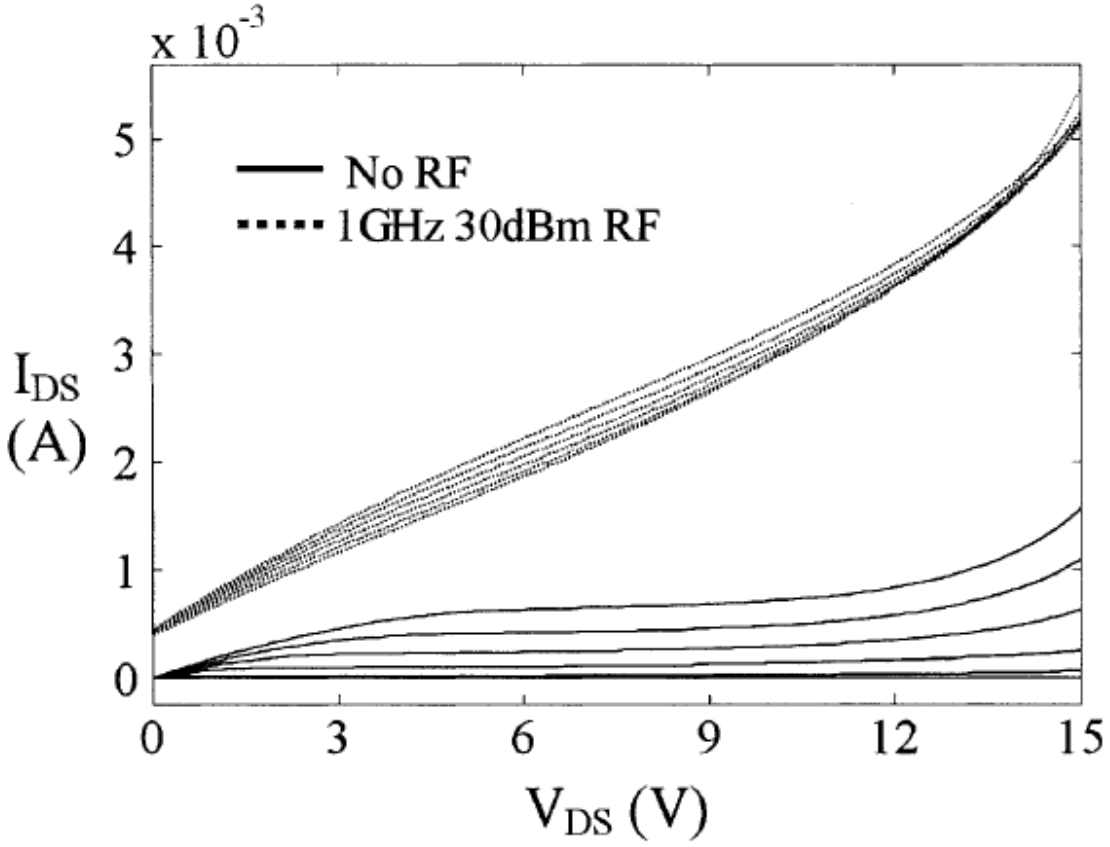


Figure 12. 30 dBm RF effects on I-V output characteristics [11]

The RF signal applied to the gate is driving the MOSFET into deep inversion to an approximately uniform channel as shown in Figure 12 [11]. Saturation is not occurring owing to the channel not pinching off and the result is a channel that acts as an ohmic resistor. The RF signal is increasing the number of holes within the oxide by forcing the holes to oscillate, increasing the probability of hole trapping. The field in the

channel region is then stronger than that produced by the drain-to-source voltage and the channel does not saturate and pinch off as expected when not under the effects of RF.

The probability of a device upset increases when the frequency of the RF on the gate matches a resonance of the target device. When a signal matches resonance, it allows the power of the field to couple into the device more efficiently. This will result in the absorption of more of the signal's energy and induce larger currents. A wide band RF signal will not couple into the device as well and would induce much smaller currents. This would not be as likely to cause RF damage to the device. Most electronic systems are vulnerable to RF in the 0.5-5 GHz range [11]. Hence this is the frequency range that will be used in this research.

III. Experimental Setup

3.1 Introduction

In order to characterize the Fairchild NDS352AP MOSFET devices, a number of different measurements needed to be conducted. The measurements included pre-characterization, RF signal on the gate only, in situ gamma cell measurements only, and the combined effects of an RF signal on the gate while being irradiated in the gamma cell.

A Keithley 4200 Semiconductor Characterization System (SCS) was used to characterize the samples. First, the pre-irradiation response of all of the selected samples was recorded in order to get baseline measurements to compare with irradiation results. RF measurements with varying frequencies and power levels and Standing Wave Ratio (SWR) tests were performed. The Agilent E8247C Signal Generator was used to perform the RF testing and the Hewlett Packard (HP) 8720C Network Analyzer was used to perform the SWR testing. Once these pre-characterization measurements were performed, the samples and experimental setup were moved to the Ohio State University (OSU) research reactor. Once there, the samples were irradiated and measured under a variety of conditions. In order to easily differentiate samples a naming convention was used which correlates the samples to the effects that they were exposed to. This convention is listed in Table 1.

Table 1. Naming convention for different experimental conditions

Sample Designation	Sample Name	RF Exposure	Radiation Exposure	RF and Radiation Exposure	5 V Gate Bias During Irradiation and Recovery
C-Control	C1	No	No	No	N/A
	C2	No	No	No	N/A
R-Radiation	R1	No	Yes	No	No
	R2	No	Yes	No	Yes
	R3	No	Yes	No	Yes
M-Microwave/RF	M1	Yes	No	No	N/A
	M2	Yes	No	No	N/A
	M3	Yes	No	No	N/A
	M4	Yes	No	No	N/A
MR-Microwave/RF and Radiation exposure	MR1	Yes	Yes	Yes	Yes
	MR2	Yes	Yes	Yes	Yes
	MR3	Yes	Yes	Yes	Yes

More details of each experiment are listed in the following sections.

3.2 Sample Preparation

After the Fairchild NDS352AP MOSFET samples arrived, they were unpackaged and stored in miniature plastic sample containers as shown in Figure 13.

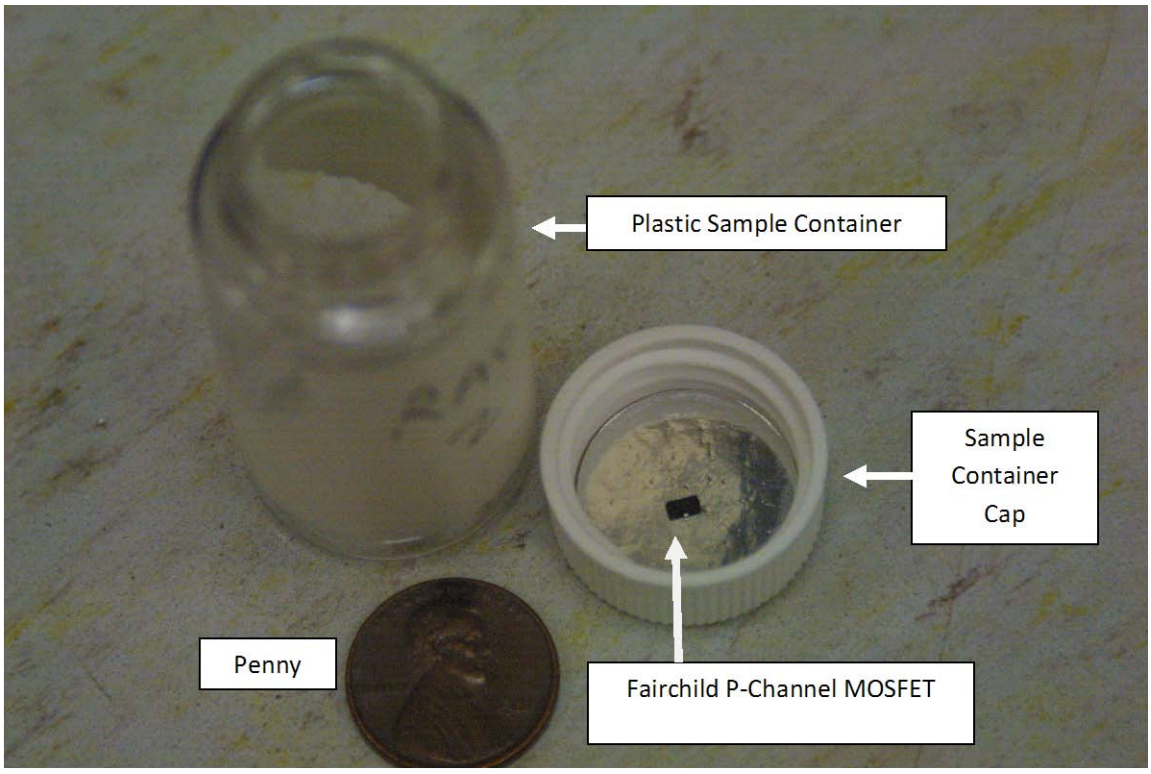


Figure 13. Sample container and MOSFET used For this research

For these measurements it was necessary to interchange MOSFETs quickly. Therefore, a solder free connection was used. In order to facilitate this need, a cradle that fit these devices and designed for use with high frequency applications was used. The cradle is a model number SOT23-3 from Emulation Technologies. Further specifications can be found in Appendix C. Emulation Technology SOT23-3 Cradle Specifications. The cradle is illustrated in Figure 14 and is shown seated in the testing platform in Figure 15.

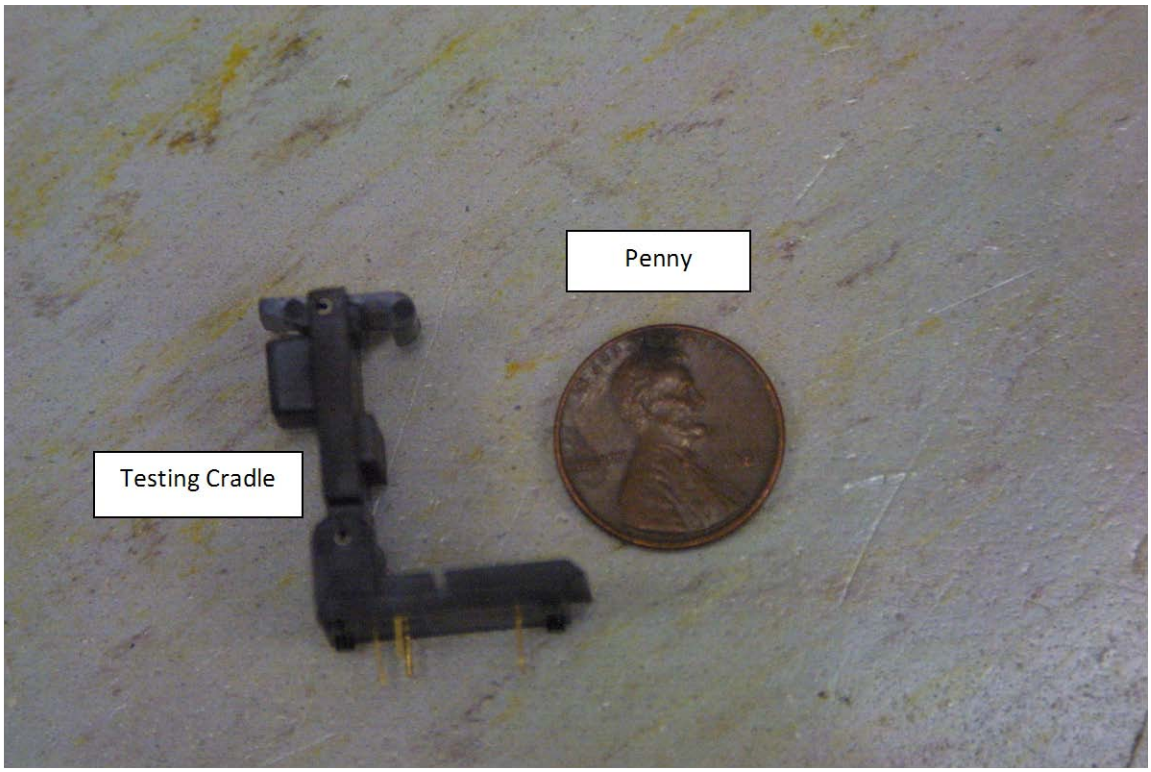


Figure 14. Cradle used to measure all MOSFETs

A testing platform was designed around this cradle as well as the SMA adapters needed for RF signal propagations and the coaxial and triaxial style BNC cabling native to the SCS. The platform is shown in Figure 15.

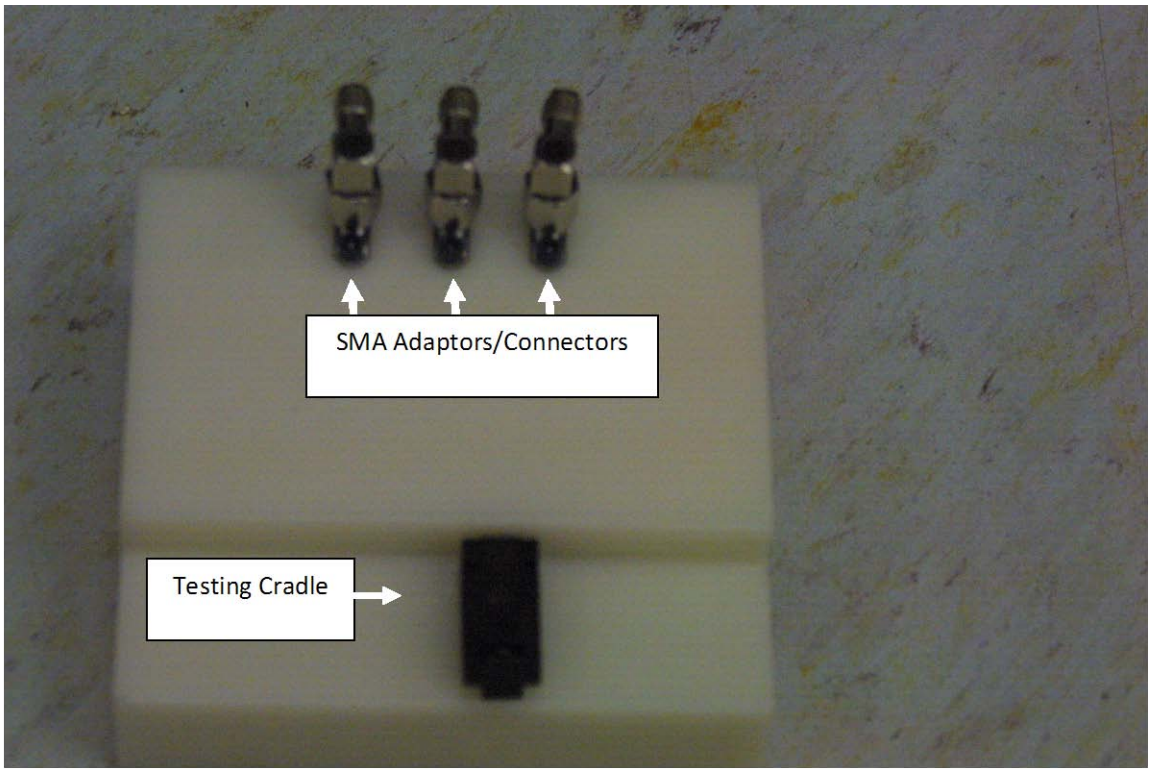


Figure 15. Testing platform with mounted MOSFET cradle used for all measurements

With this platform, the samples could be connected to any of the systems needed to conduct measurements for this research.

3.3 I-V and Threshold Voltage Procedures

The SCS was connected to the testing platform by using a custom built SMA-to-BNC adaptor box consisting of the necessary adapters, an aluminum hobby box, wiring, and solder. A picture of the conversion box is shown in Figure 16.

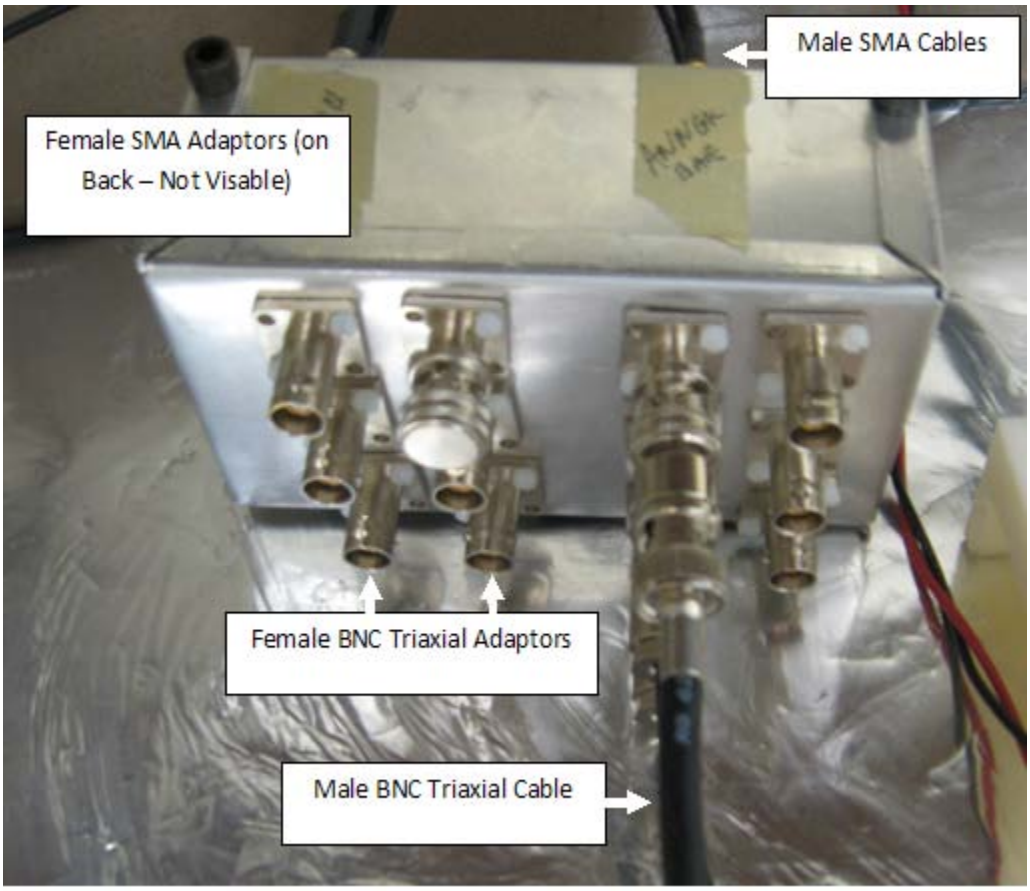


Figure 16. Conversion box used to connect cables from RF signal generator and Keithley 4200 to the testing platform

For both measurements, a program was written and used to automate the collection of data. For the I-V measurement, the gate voltage was set to a voltage, usually -2 V, and then the voltage on the drain was changed, sweeping between 0 and 1 V at 0.01 increments. The source had no voltage applied during this measurement. While this was occurring, the drain current, I_{DS}, was measured and plotted against drain to source voltage, V_{DS}. The gate voltage was incrementally increased by steps of -1 V and the curves are plotted. The result resembled the results illustrated in Figure 3.

For the threshold voltage measurements the gate voltage was swept between -2 and -5 Volts at increments of -0.01 V. A constant bias of -2 V was applied to the drain and the source was left with no bias. While sweeping the drain current, I_{DS}, was measured and plotted against the gate voltage, V_G. The standard curve produced should be similar to that shown in Figure 17. Experimentally the threshold voltage was obtained by extracting the x intercept of the I_{DS} vs V_G data shown in Figure 17. The curve, however, does not lend itself to a straightforward calculation of threshold voltage. In order to measure the threshold voltage consistently every time, the following method was used. First the midpoint was found on the S shaped curve, the program then searches for the value which is closest to this value in the actual data. The changes in I_{DS}, dI, and V_G, dV, were computed and the ratio of the two was stored in an array. Using the midpoint and the slope, dI/dV was found and used. Using the point slope equation of a line, given in the equation (12), a line was plotted and the x intercept was taken as the measured threshold voltage, V_{Tmeas}.

$$I_{DS} - I_{DSo} = \frac{dI}{dV}\left(V_G - V_{Go}\right) \tag{12}$$

The point is given by the Cartesian coordinate (V_{Go},I_{DSo}) and dI/dV is the slope. An adjustment was needed to account for the bias on the drain. The following equation adjusts the measured threshold voltage:

$$V_T = V_{Tmeas} - \frac{V_D}{2}. \tag{13}$$

Where V_T is the adjusted threshold voltage and V_D is the drain voltage used in the measurement. Using this adjustment would yield a threshold voltage of -0.83 V for the NDS352AP MOSFET if used with the measurements in this work. Fairchild semiconductors reports the threshold voltage of the MOSFET used in this work should be -1.7 V. This adjustment was not used for this work due to the large discrepancy it produced when compared to the manufacturer reported threshold voltage. Figure 17 shows an illustrative example of the output graph and threshold voltage computational method.

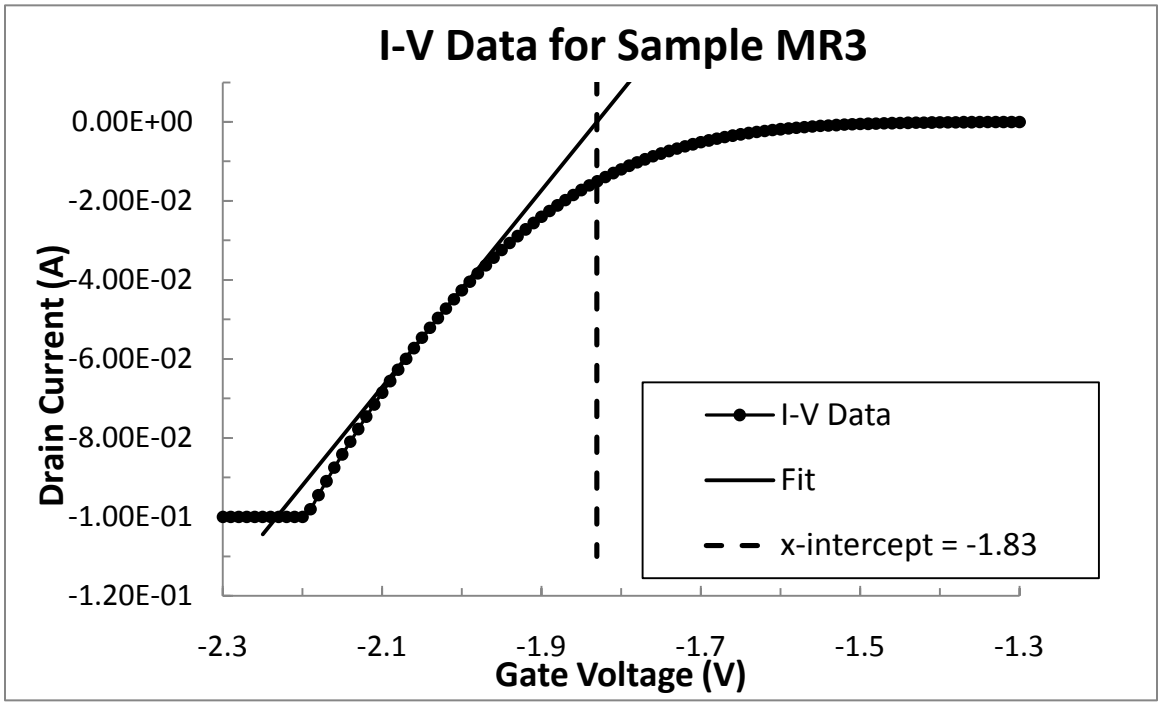


Figure 17. Example I-V curve used to calculate threshold voltage

This method was used to compute all threshold voltage measurements. Each MOSFET was characterized using the I-V and threshold voltage measurement techniques, outlined in this chapter. No less than five measurements of each sample were taken. The threshold voltage derived from this threshold voltage computational technique was averaged and the standard deviation was computed for each set. All MOSFET results were then averaged and the standard deviation was calculated by taking the square root of the sum of the variances (the standard deviation squared). The average threshold voltage of all samples was found to be -1.827 V. More importantly, the maximum standard deviation of any given sample (measured multiple times) was found to be 0.0005020 V. The standard deviation will be assumed to be the error of this measurement technique, which is approximately 0.02% per standard deviation. The error in this measurement technique is so minimal that it does not affect any reported threshold voltage measurements. All threshold voltage measurements are reported to three decimal places.

3.4 RF Experimental Procedures

In order to ensure that an RF signal is reaching the MOSFET, a SWR test was performed using a Hewlett Packard 8720C Network Analyzer. The network analyzer measures the sample by varying the frequency range on the sample and plotting the transmittance against frequency. The resulting values of the transmittance clearly show which points have the most resonant coupling and which points are reflecting most of the signal. This measurement was performed using frequencies ranging from 1 to 5 GHz and 1 to 10 GHz. It was also repeated while the leads were attached to the gate and drain as well as to the gate and source. Both measurements were expected to be the same but

were both performed in order to be thorough. The results of this measurement are shown in chapter 4.

Once the optimum transmittance was known, an Agilent E8247C signal generator was used on the four MOSFETs chosen for RF exposure only. The MOSFETs were exposed to a frequency of 2.77 GHz at power levels of 1 dBm, 7 dBm, and 14 dBm. A bias tee was used to combine the direct current (DC) from the SCS and the alternating current (AC) from the signal generator. The bias tee allowed measurement of the sample while keeping the RF constantly applied to the gate. Results of this measurement are shown in chapter 4 and further explained.

3.5 Gamma Irradiation Procedures

Once the RF vulnerability and the initial threshold voltages were known, irradiation in a gamma cell was performed using an identical measurement system. A platform that can be raised and lowered by an electric lift was used to insert and remove the testing platform from exposure to the gamma source. The MOSFET was mounted in the cradle and lowered into the gamma cell with 25 feet of SMA cabling connecting the testing platform to the SCS. A picture of the gamma cell and testing platform is shown in Figure 18.

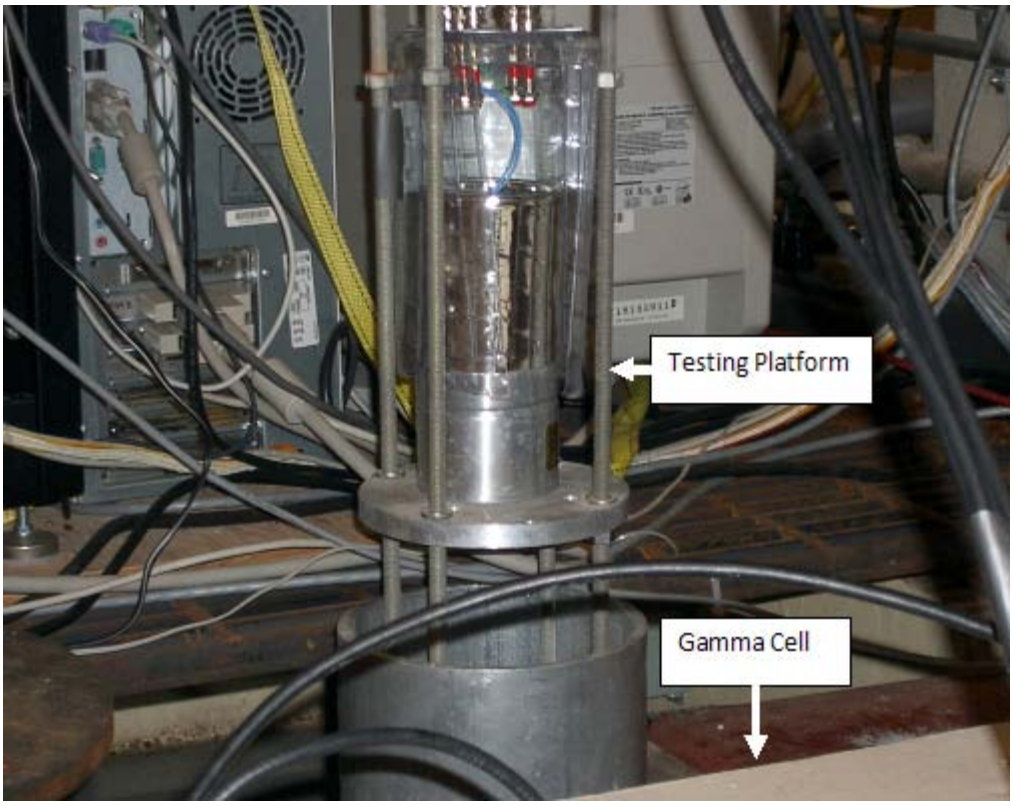


Figure 18. Gamma cell at the OSU research reactor complex

The exposure rate, as a function of position, as of 4/6/2010 of the gamma source is shown in Figure 19. The dose rate of the gamma source at the time of the experiment was 66.7 krad/hr (1111.67 rad/min) [19]. This data is based upon calibrated dosimetry measurements performed on Jan 28, 2002. The dose rate is calculated based on the theoretical decay of the radioactive source from the calibration date.

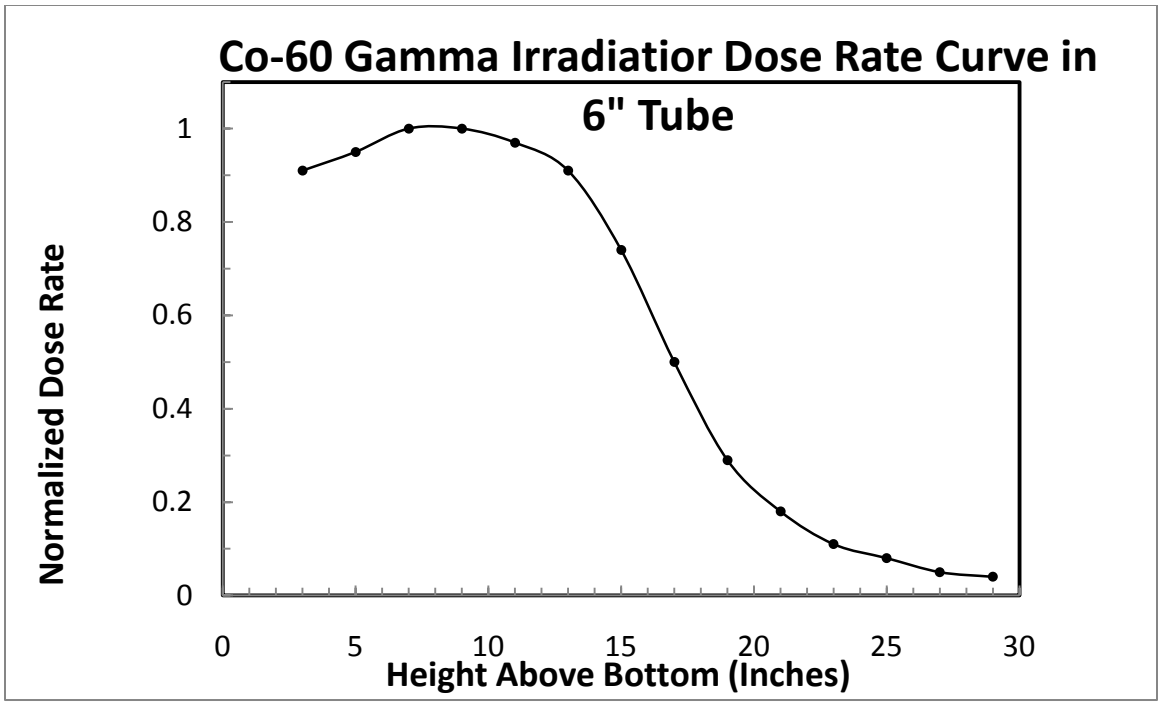


Figure 19. Dose curve for gamma irradiation cell at OSU's research reactor facility [19]

Samples were irradiated and measured in-situ for variable amounts of time. This procedure was used because threshold voltage damage is a function of total dose (which is higher for longer exposure times). During and after irradiation, MOSFET R2 had a +5 V gate bias while sample R1 did not. For clarity, +5 V gate bias is used to refer to the bias on the gate while the sample is not being measured. Measurement requires the bias on the gate to change. Therefore, a DC power supply providing +5 V on the gate was applied to the sample and removed while measurements were taken. Measurements require a maximum of 60 seconds so the time the sample is removed from the power supply is minimal compared to the overall irradiation and anneal time. The gate bias is assumed to be constant during irradiation and annealing.

The in situ gamma irradiation measurements established a threshold voltage damage curve which allowed for the comparison of damage effects from gamma radiation only and gamma radiation with a RF signal applied to the gate. MOSFETs MR1 and MR2 were irradiated with a gate bias of +5 Volts and a 2.77 GHz RF signal at 14dBm power. The bias and RF signal ideally should be constant during recovery but were interrupted for an hour while the setup was moved to another location for monitoring. The results at the time indicated a need for a third set of measurements. During the third set of measurements MOSFET R3 did not have RF applied to the gate but had a +5 V bias during irradiation and throughout its recovery period. MR3 was irradiated with the same RF signal as earlier samples and kept under a +5 V bias and RF after it was removed for its entire recovery time.

IV. Results and Analysis

4.1 Results From I-V and Threshold Voltage Pre-characterization Measurements

The pre-characterized MOSFETs exhibited the expected I-V relationships as shown in Figure 17 of chapter 3. The samples were all measured before performing any irradiation or RF experiments. The threshold voltages before any bias, gamma, or RF effects are all plotted in Figure 20.

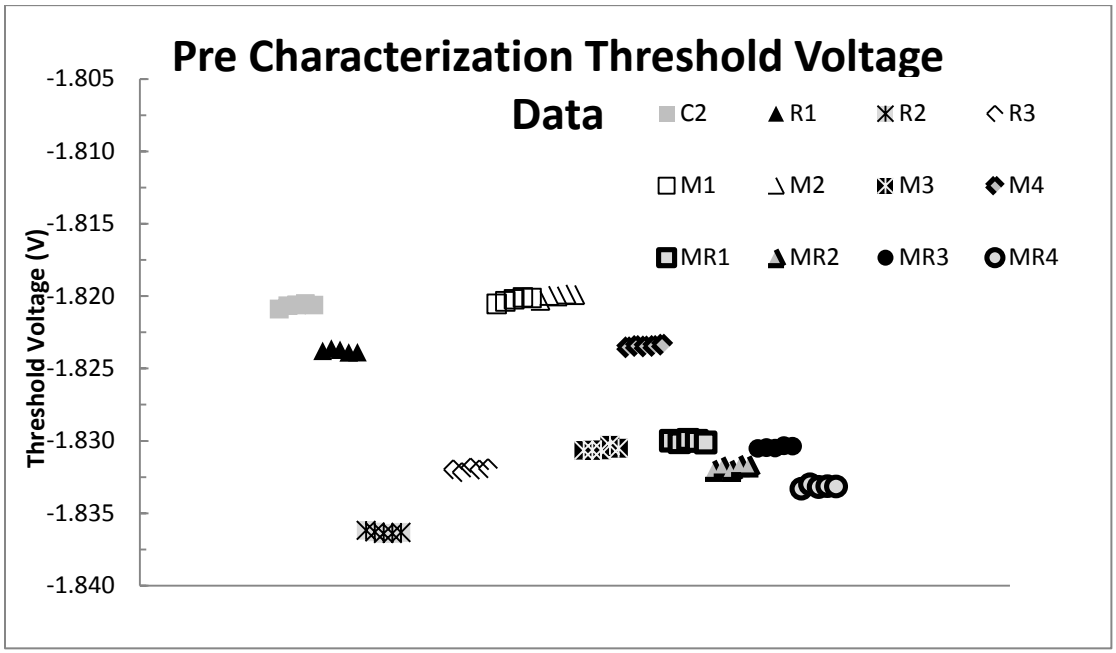


Figure 20. Pre-characterization threshold voltage measurements

The expected threshold voltage provided by the manufacturer is -1.7 V. The measured results ranged from -1.791 V to -1.852 V. The average value of these measurements is -1.827 V with a standard deviation of 0.0126 V. The maximum percent difference between the minimum and maximum value is 3.25%. The difference in manufacturer

value to my measured value is likely the method of calculation but could also be due to lab condition and temperature differences. Due to the lack of spread in the values it will be assumed that the device operates at -1.83 V at room temperature.

For the I-V data the expected theoretical shape modeled in Figure 3 was not observed. The saturation region was not observed in the I-V measurements. This problem was caused by the SCS hitting compliance at 0.1 A during the measurement. Even though the saturation regions are not present, the linear region can be seen. A comparison, of two samples which exhibited the largest difference, is shown in Figure 21.

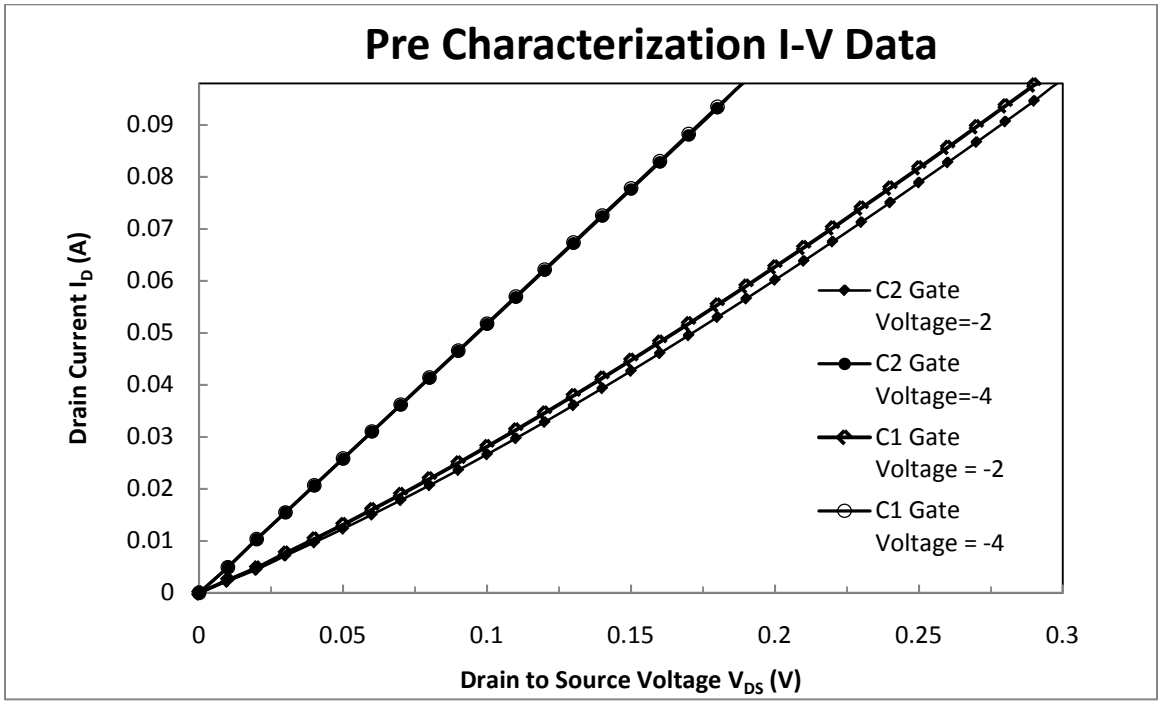


Figure 21. Pre-characterization I-V data

By selecting the samples demonstrating the largest differences, the upper and lower bounds of all measurements can be shown. This demonstrates the largest deviation

in the measurements. In the -2V gate voltage curves the linear region between sample C1 and C2 shows a maximum 7.46 % difference at 0.28 V. The average of all points with a -2 V bias, however, is only 1.46%. This difference diminishes to a maximum of 1.81% at -3 V gate bias and 1.07% at a -4 V gate bias. In Figure 21, the C1 and C2 data for a -4 V gate bias overlaps so much that the points are barely distinguishable. As the gate voltage increases the linear region of the device has a greater slope and the difference in I_{DS} at a fixed gate voltage reduces. The measurement differs as the gate voltage changes owing to the strength of the electric field produced by the gate bias. As the negative bias increases, more holes are attracted to the channel region, increasing the hole density in the channel region. These holes produce a stronger electric field within the channel. Therefore, the drain to source voltage must be higher to pinch off the channel. For a higher negative gate bias, more drain to source current flows through the channel for a given voltage and the saturation (or pinch off) occurs at a higher drain to source voltage.

4.2 Results of High Power Microwave Measurements

For the SWR measurement, the goal was to determine the optimum transmittance of the experimental cradle setup in order to ensure that a RF signal was coupling into the MOSFET device. The results of these measurements are shown in Figure 22, Figure 23, and Figure 24.

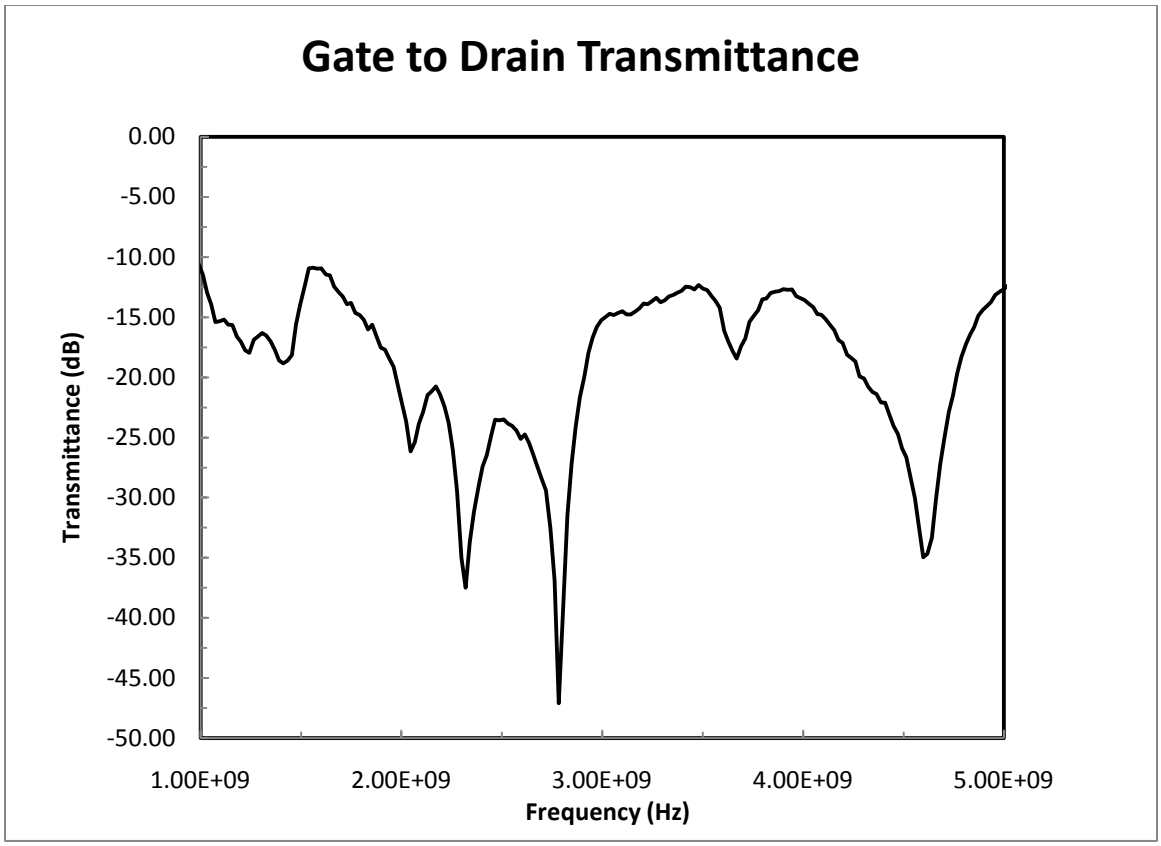


Figure 22. Gate to drain transmittance of RF Signals into the experimental cradle setup

From Figure 22 it is evident that there are 2 major transmittance frequencies shown, 2.32 GHz and 2.77 GHz. In order to select a frequency the gate to source transmittance was also measured and is shown in Figure 23.

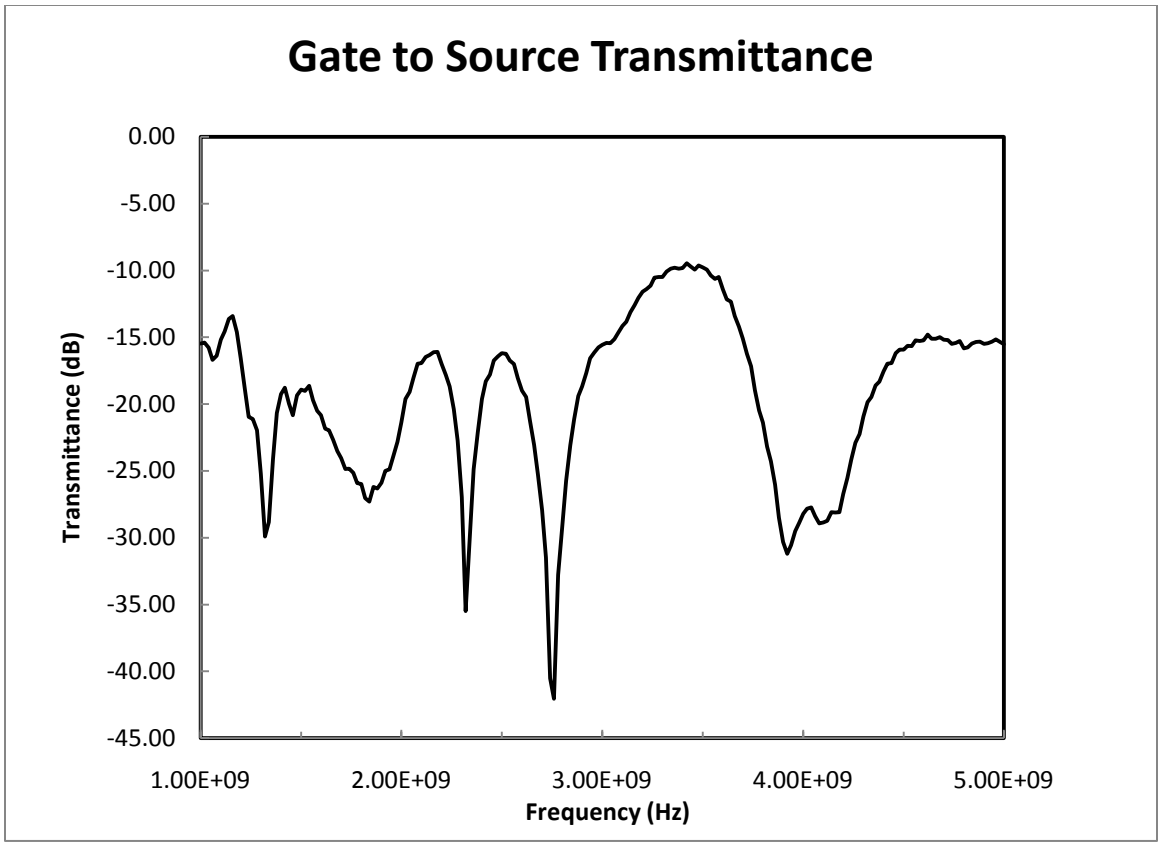


Figure 23. Gate to source transmittance of RF signals into the experimental cradle setup

The gate to source test yielded data similar to that of the gate to drain, as expected. The two optimum frequencies are 2.32 GHz and 2.77 GHz. At 2.77 GHz the transmittance is greater, therefore, that was chosen as the best device frequency for resonant coupling. In order to be thorough the test from 1 GHz to 10 GHz is shown in Figure 24.

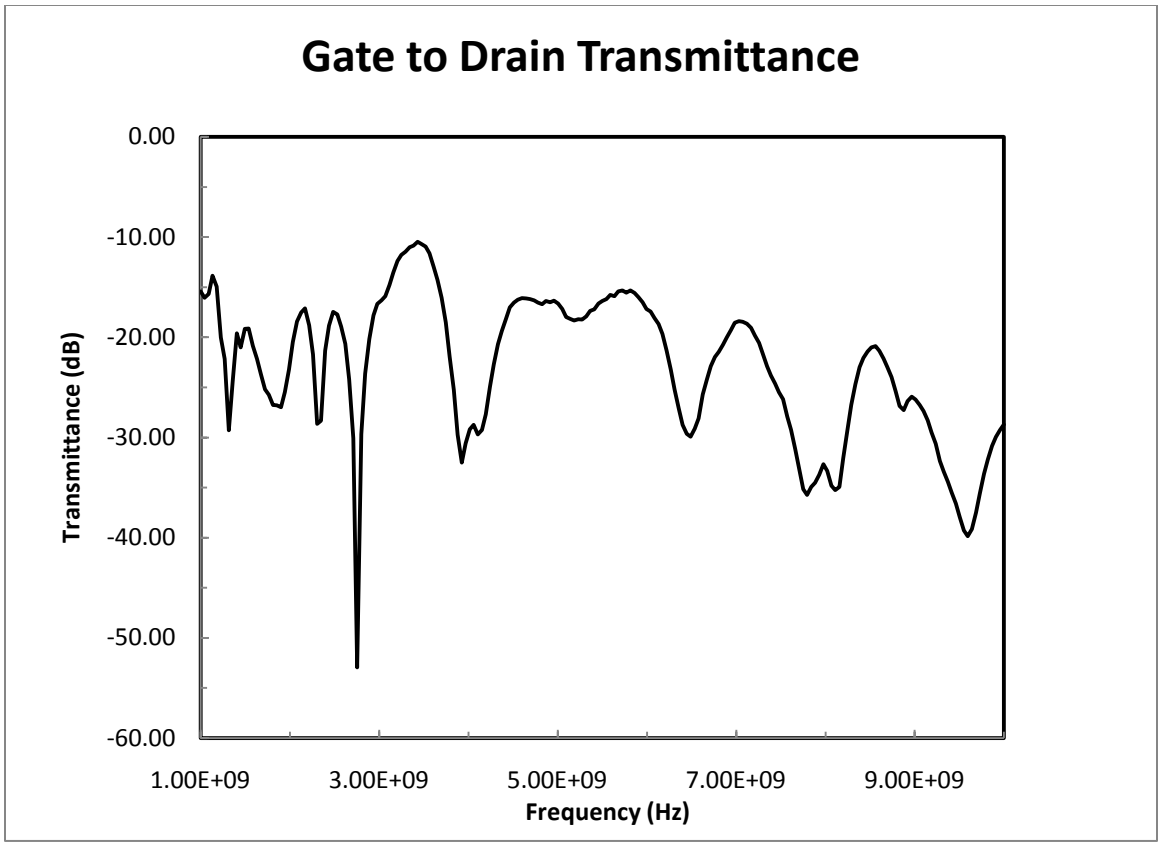


Figure 24. Gate to drain transmittance of 1 to 10 GHz RF signal sweep into the experimental cradle setup

The data shows that the largest transmittance point is in fact at 2.77 GHz. These tests contributed to the selection of 2.77 GHz as the optimum frequency to penetrate the cradle contacts. In all configurations and frequency ranges 2.77 GHz produced the most transmittance. Therefore, 2.77 GHz was assumed to be the resonant frequency of the device. With the device resonant frequency known further RF experiments, as outlined in the chapter 3, were performed.

Using the signal generator, the samples were exposed to varying power levels of the 2.77 GHz signal in order to determine any effects of RF on the sample separate from the radiation. The threshold voltage results are shown in Figure 25.

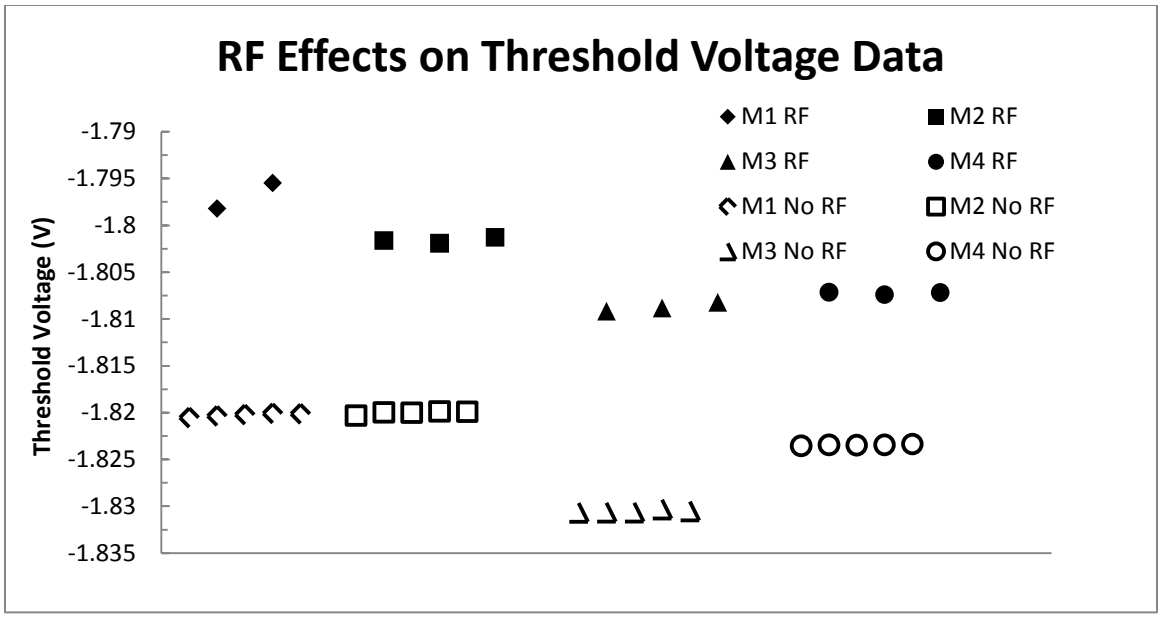


Figure 25. 2.77 GHz RF applied to the Samples at varying power levels

The first point of each sample data set is at a power of 1 dBm. The second point of each set is at a power of 7 dBm. The third point of each set is at a power of 14 dBm (for the M1 series the 14 dBm measurement was omitted as an outlier). It is clear in the data that the power level is not influencing the magnitude of the threshold voltage. The threshold voltage data exhibits an upward shift of 1.57% from the average initial value of -1.83 V. The average value of the sample under RF at all power levels is -1.804 V with a standard deviation of 0.0047 V. The threshold voltage shift is very small. Temperature differences or other minor changes in the environment could also be responsible for this change. In theory, the RF could induce currents that could force trapped oxide holes to the interface. Fewer holes within the oxide would increase the value of the threshold voltage. While the change is small, a trend of increasing threshold voltage is observed in Figure 25.

Under the same conditions as the threshold voltage tests, the I-V data was also collected and plotted. Figure 26 shows the results from these measurements.

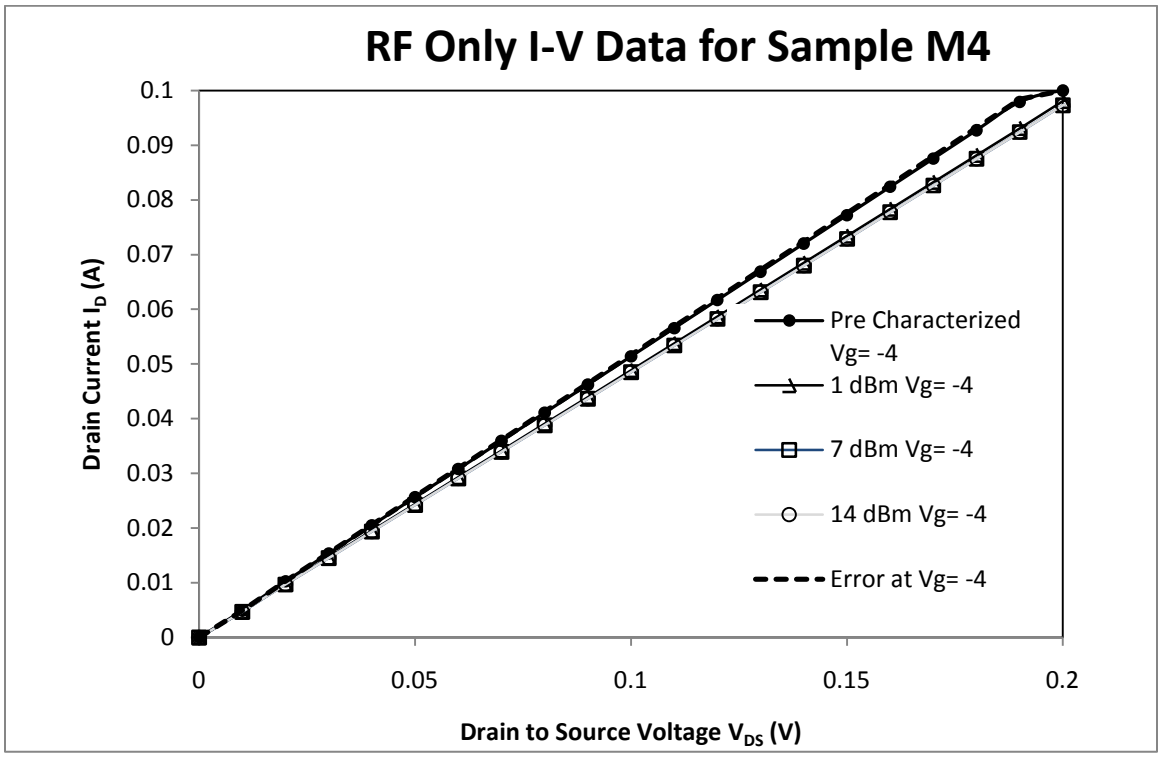


Figure 26. RF effects on the I-V characteristics of sample M4

The power level of the RF signal provides no discernable effect on the I-V characteristics when -2 V is applied to the gate. The RF signal shows up to a 5.95% shift in the I-V curves, when -4 V is applied to the Gate, from those measured in the initial characterization measurements. The percent shift is higher than the shift in the control samples at -4 V bias. The RF is expected to shift the linear region to the right and lower for a p-channel device based on the previous work of Kim shown in Figure 11 of chapter 2. This measurement also conflicts with the threshold voltage measurements which

showed a trend of increased threshold voltage. The behavior exhibited in Figure 26 implies a decrease in threshold voltage. The measurements shown in Figure 25 and Figure 26 cannot exist simultaneously. More measurements are required to resolve this discrepancy.

4.3 Gamma Irradiation Results

For the samples that were irradiated without RF, two experiments were performed. These were to compare the effects of bias on the threshold voltage shift during irradiation. Before exploring those results a plot of the I-V characteristics as a function of radiation damage at five different irradiation times is shown in Figure 27.

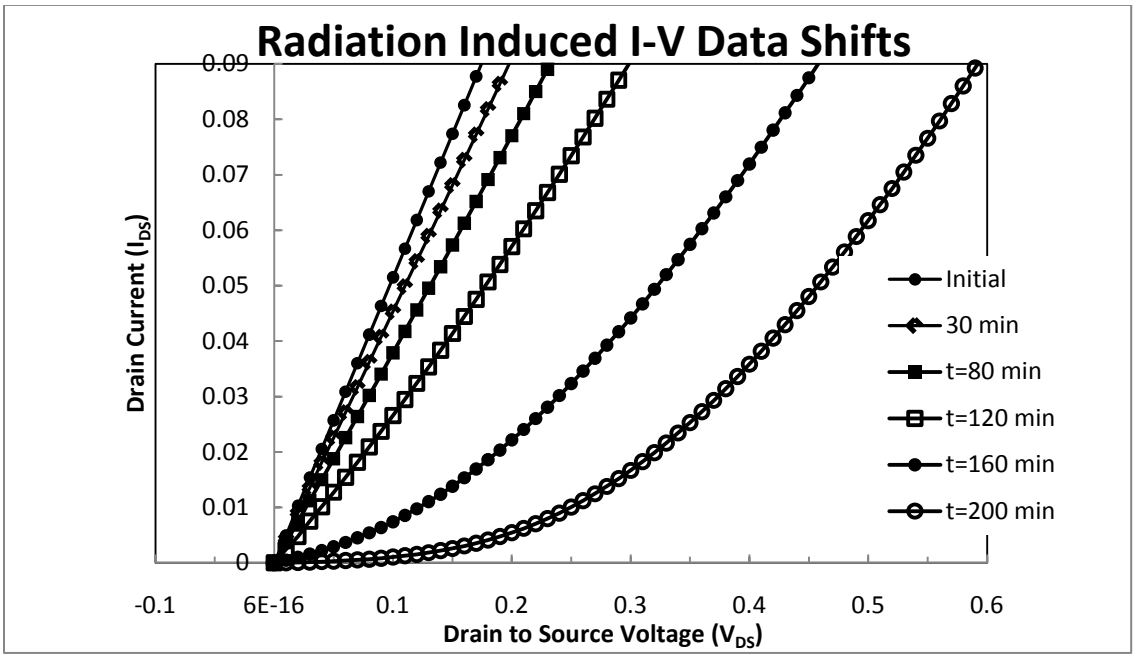


Figure 27. Effects of radiation on MOSFET output characteristics with -4 V applied to the gate

The current in the I-V curves tends to shift to the negative direction for the same V_{DS} as irradiation time increases. This behavior is typical of p-channel MOSFETs owing to radiation induced oxide trapped holes. Hughes and King suggest that distortions in post irradiation I-V curves could be due partially to lateral non-uniformities of the interface and oxide trapped charges [9]. Oxide trapped charge explains the behavior in Figure 27 well owing to more voltage being required to drive the same current through the channel. As the charges build up within oxide a higher field would be required to move the same current through the channel region. As radiation damage increases, the device is not turning on until more voltage is applied to the drain. The channel region is behaving as if it is pinched off or not conductive until more voltage is applied to the drain. The irregular channel behavior is responsible for the non-linearity observed in Figure 27.

A measurement of the samples under the effects of gamma radiation were performed. Sample R1 had no applied bias while sample R2 had a +5 V bias applied to the gate. The results are shown in Figure 28.

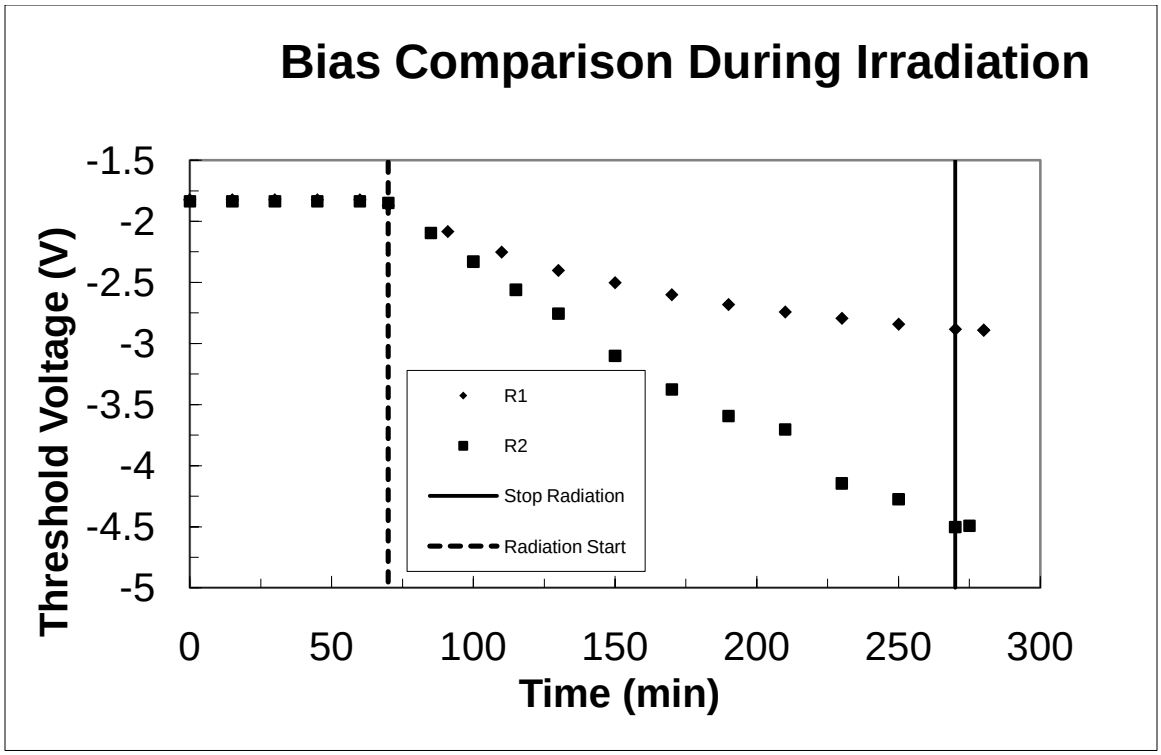


Figure 28. Effects of gate bias on threshold voltage during irradiation

Irradiation under a positive gate bias causes higher densities of interface traps and trapped oxide charge than under negative gate bias [25]. The positive gate bias creates an electric field, which pushes holes to the interface and pulls electrons away. During irradiation, holes and electrons are created within the oxide layer. The positive gate bias accelerates the holes toward the interface. The electrons are attracted to the gate, exiting the oxide more quickly than without the bias and have a lower probability of recombining with the holes that are trapped in the oxide. A lower recombination rate results in more holes left within the oxide. Also, any de-trapped holes within the oxide accelerate more quickly to the interface and then tunnel through. The process of a holes tunneling to the channel region forms interface traps.

Charge yield, transport, and trapping are all bias dependent processes [15]. As a result of the bias dependence, the change in threshold voltage also depends upon the gate voltage applied during irradiation. In the case of p-channel MOSFETs, the magnitude of the threshold voltage increases when a positive bias is applied to the gate during irradiation. This behavior is illustrated in Figure 28. The magnitude and rate of change of the threshold voltage are of interest. By calculating the rate of threshold voltage change one can then determine when to stop irradiating the target in order to induce a precise threshold voltage change. This assumes the sample is not reaching saturation and is linear.

In the case of the samples measured in Figure 28 the biased sample exhibited a much higher rate than the unbiased sample, as predicted. The threshold voltage damage rate of the unbiased sample was measured and averaged to be -0.0054 V/min with a standard deviation of 0.0028 V/min. The threshold voltage damage rate of the biased sample was measured to be -0.014 V/min with a standard deviation of 0.0048 V/min. This rate is 2.64 times as large as the unbiased counterpart. Furthermore, the rates of all other samples irradiated were measured and averaged to be -0.016 V/min with a standard deviation of 0.00163 V/min. The +5 V bias damages the sample 2.98 times more quickly than the unbiased sample, assuming a linear relationship.

NAVSEA Crane evaluated the total ionizing dose performance of the NDS325AP p-channel MOSFET [24]. The specifications of the test were drafted by Christian Poivey of NASA. Each Fairchild MOSFET tested was exposed to gamma irradiation at a dose rate of 53.15 rad/min until the sample had a total Dose rate of 50,000 rad [24]. In order to compare to the data in this work the total dose was converted to a time. The time of

irradiation in the NAVSEA measurements was longer; however, the dose rate was lower. In order for a comparable examination of the data, the NAVSEA data was converted from total dose to time that was scaled to fit with the times used for this work. This ensures that the effects can be illustrated and analyzed on the same graphs. Each sample was irradiated under a +5 V bias to the gate. Each NAVSEA sample was annealed for 168 hours under the same gate bias and measured again [24]. The threshold voltages were then plotted and compared. Control samples were also measured and were not exposed to radiation or gate bias. Note throughout the rest of the document tests performed by NAVSEA will be referred to as NASA tests, because they are presented as such on NASA's data site. The data of the unbiased sample is displayed in Figure 29.

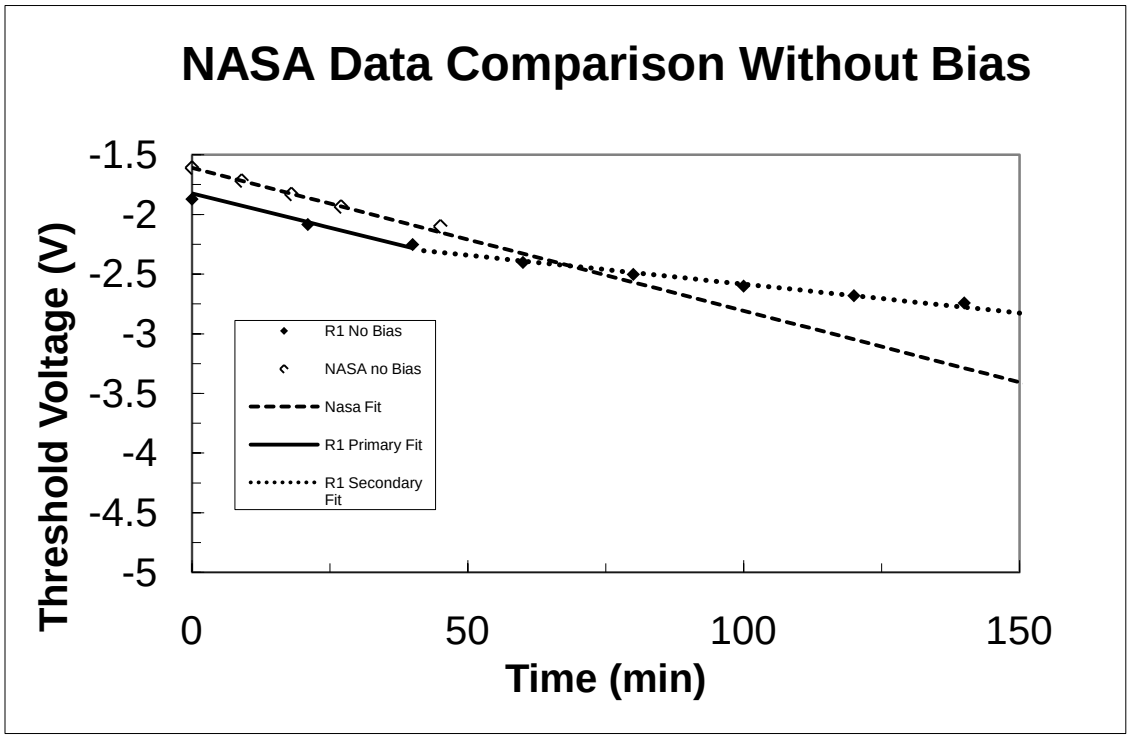


Figure 29. Comparison of unbiased measurements from this work to NASA measurements

The rate of change of threshold voltage in the unbiased NASA tested sample was measured and averaged to be -0.0119 V/min with a standard deviation of 0.00900 V/min. The first three data points from MOSFET R1 agreed well with the NASA data. The primary data fit, defined as when both data set times overlap; averaged -0.0115 V/min. The primary data exhibited a slope that was 4.00% less during irradiation when compared with the NASA data. The secondary fit does not provide a useful comparison because there are no NASA data points to compare with. The secondary fit's threshold voltage shifted at an average rate of -0.00484 V/min with a standard deviation of 0.00622 V/min. Differences between primary fit and the NASA data can be attributed to differences in method of measurement of the threshold voltage or manufacturing conditions. The secondary fit exhibited a slope that was 59.9% lower than the slope of the NASA samples. The results of this research agree well with the NASA tested samples assuming a secondary process when no bias is applied. The later data has a greatly reduced slope suggesting the onset of a secondary process.

Saturation during irradiation is largely due to the recombination rate increasing as the number of trapped oxide charges increases [1]. This produces an increased internal space charge which reduces the net internal field. However, the number of hole traps located within the oxide is limited. Neither the trap filling nor recombination fully explains the saturation phenomenon. The damage tends toward a saturation point which would begin to cause threshold voltage shifts to exhibit non-linear behavior during irradiation. Boesch et al. suggest that there could be multiple processes involved in modeling radiation induced MOSFET damage [1]. In most cases, the threshold voltage

shift during irradiation is assumed to be linear. This data does not support a linear fit, and shows an influence of saturation around 50 minutes into the irradiation.

For the biased samples a similar comparison was made and the results are shown in Figure 30.

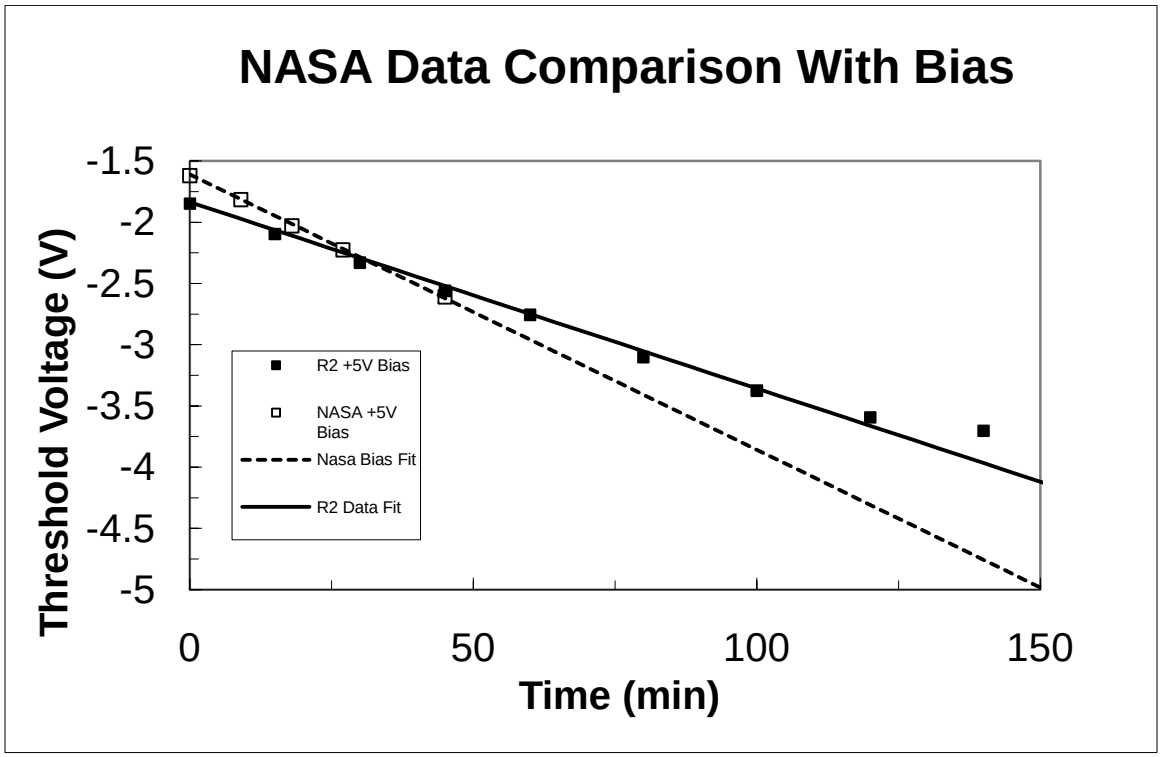


Figure 30. Comparison of biased measurements from this work to NASA measurements

The measured average rate of threshold voltage change measured by NASA was -0.0225 V/min with a standard deviation of 0.00025 V/min. The slope of the threshold voltage for MOSFET R2 was 28.8% higher at -0.0165 V/min with a standard deviation of 0.00163 V/min. Again, the deviation of the NASA data points was small but there are fewer data points. Another explanation for the lack of correlation could be the number of points taken and the details of the experiment. The NASA experiment does not establish

the profile for higher dose rates. While both samples are exposed to relatively low dose rates (1111.67 rad/min and 53.15 rad/min) they may still require higher total doses to establish the device behavior. When dose rates are too low annealing of the sample can occur while being irradiated. Annealing would slow the rate of threshold voltage change, reducing the magnitude of the slope. The annealing effect is assumed to be negligible and is not observed in this work. The slope of the threshold voltage change in this work is less than the slope reported by NASA despite a much higher dose rate.

The data taken with bias on the gate was fit linearly. The NASA experiments do not reach saturation and exhibit a linear does relationship. The data taken in this work extends to higher total dose and, therefore, could reveal secondary processes that affect the magnitude of threshold voltage change. The later data could also be statistical outliers. The data in this work does not agree with the NASA data, especially at earlier points. However, the data is more linear throughout when compared with the unbiased data in Figure 29.

Non-linear behavior was not attributed to the data in Figure 30 even at the much higher dose rates. The influence of a secondary saturation process on the MOSFET during irradiation seems to correlate with the applied gate bias. Further studies are needed to investigate this relationship. Measurements with and without bias during irradiation would be needed. Irradiating samples long enough to observe the effects of saturation without bias could provide a base comparison for other measurements. Then varying the magnitude of the bias on the MOSFETs during irradiation could show the correlation of bias on device saturation during irradiation. These results could lead to a

better understanding of the effects of gate bias on the saturation of p-channel MOSFETs during irradiation.

4.4 RF during Gamma Irradiation Results

In order to examine the effects that RF has on the sample during irradiation samples were irradiated with and without RF. The results of these experiments are shown in Figure 31.

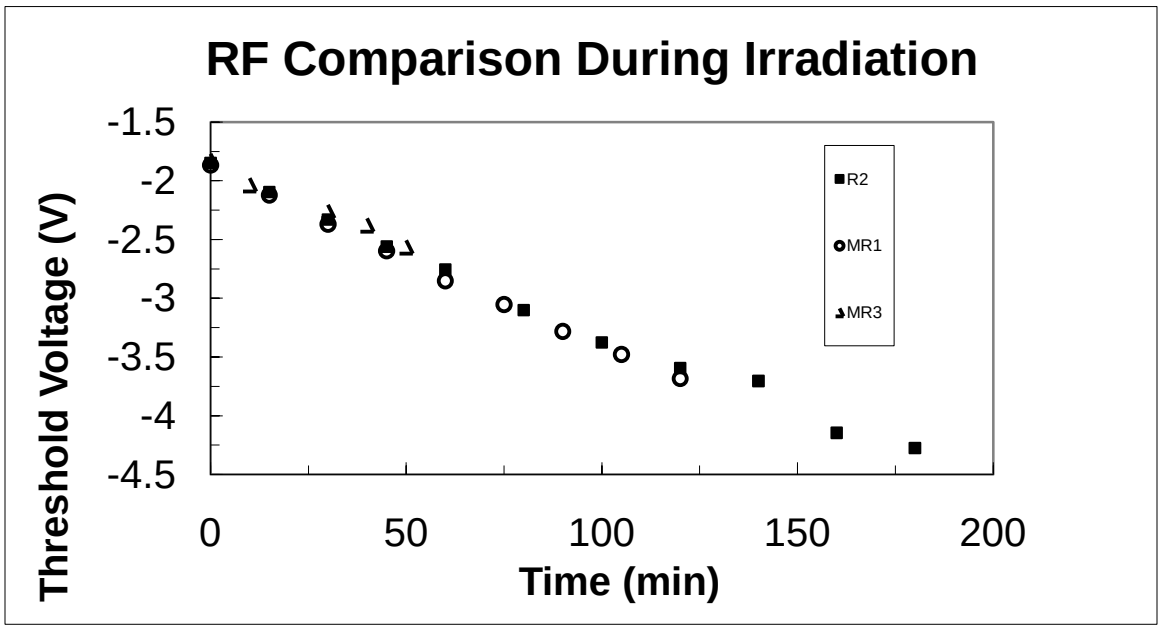


Figure 31. Comparison of biased samples during irradiation with and without RF

In the above data sample MR3 was removed from the gamma source at 50 min, MR1 at 120 min and R2 at 200 min. The cited rate of threshold voltage change of sample R2 has been given previously as -0.0165 V/min with a standard deviation of 0.00163 V/min. The rate of threshold voltage damage of MR1 was calculated to be -0.0151 V/min with a standard deviation of 0.0016 V/min. The rate of threshold voltage damage of MR3 was

calculated to be -0.0153 V/min with a standard deviation of 0.0048 V/min. The RF signal on the gate increases the magnitude of threshold voltage change by 7.2%. The RF signal on the gate seems to be causing more threshold voltage damage than when the MOSFET is being irradiated without the RF. However, the behavior within the measurements looks as though it could be statistical deviation so no definite trend is established. Not enough samples were irradiated to see if the shift would fall within the error of the measurement.

4.5 RF during Anneal Results

As a final comparison the samples annealing under bias were compared with and without RF. The long term anneal results of this comparison are shown in Figure 32.

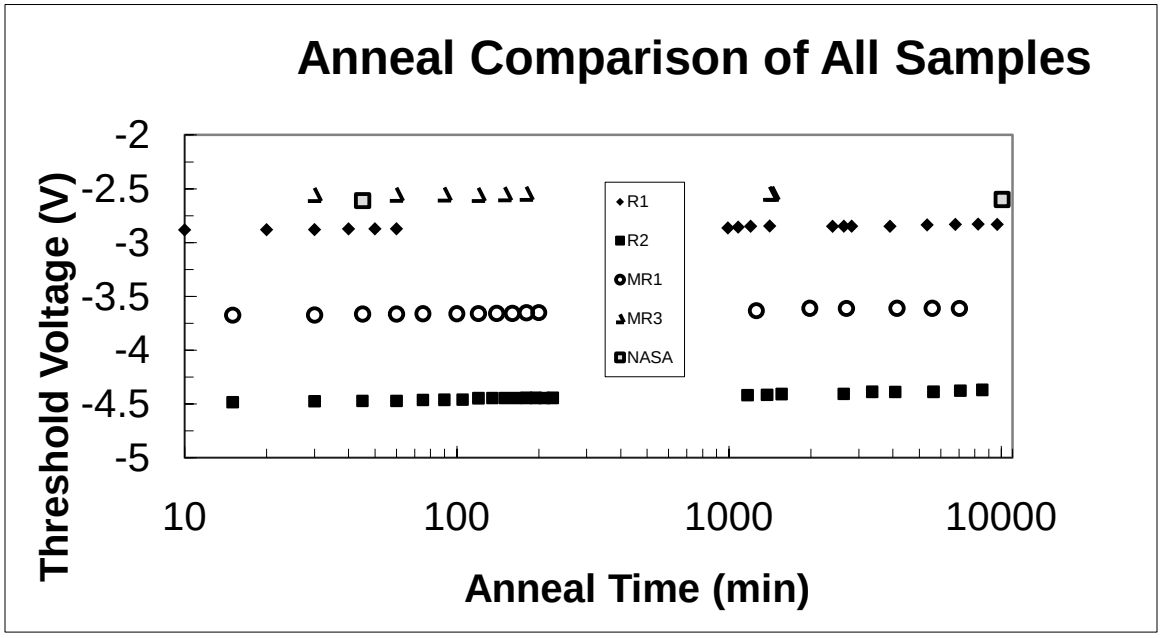


Figure 32. Anneal comparison of all samples

Note that R1 did not have bias or RF signals applied to the gate during irradiation or recovery. R2 and NASA data were biased during irradiation and recovery. MR1 and MR3 were biased and under the effects of RF during irradiation and recovery. The threshold voltage damage rates for each sample as well as the recovery rates are compiled in Table 2.

Table 2. Compiled threshold voltage changes

Sample	Avg. Threshold Change During Irradiation (V/min)	St. Deviation of Threshold Change During Irradiation (V/min)	Avg. Threshold Decay During Annealing (V/min)	St. Deviation of Threshold Decay During Anneal (V/min)
R1 - Unbiased	-0.01150	N/A	-7.10E-05	1.61E-04
R2 -Biased	-0.01654	0.00163	-1.13E-04	2.86E-04
R3- Biased	-0.01701	0.00159	2.78E-05	2.28E-04
MR1 - Biased	-0.01514	0.00161	-1.12E-04	1.66E-04
MR2 - Biased	-0.01835	0.00202	7.54E-05	6.77E-04
MR3- Biased	-0.01531	0.00483	-1.13E-04	1.73E-04
NASA- Biased	-0.02248	0.00025	-1.65E-06	8.10E-07

A comparison of the averaged rates and compiled standard deviations are shown in Table 3.

Table 3. Average threshold recovery rates with and without RF

Radiation Rates (V/min)			Anneal Rates (V/min)		
	No HPM	HPM		No HPM	HPM
Avg	0.015224	0.01634	Avg	-4.3E-05	-5E-05
St. Dev	0.002522	0.001751	St. Dev	0.0004	0.000339

The data indicates that the recovery rates of these samples is very slow. These samples also exhibit a standard deviation that makes determining precise rates of threshold

voltage recovery difficult. The unbiased samples are expected to recover more slowly than with a bias applied to the gate. This is due to the electric field of the gate bias forcing holes out of the oxide more quickly. Holes exiting the oxide at an increased rate will result in threshold voltage recovering more quickly. Expedited threshold voltage recovery when the gate is biased is well documented [15]. However, the increased recovery rate was not observed in these measurements. The MOSFETs could have numerous traps within the oxide layer far from the interface (also called deep oxide traps) or damage in the gate region. This would explain the inability of trapped oxide charges to move out of the oxide.

Gamma irradiation of a sample under the effect of a RF signal on the gate is not well understood. The RF signal on the gate did not produce observable effects on the post irradiation threshold voltage recovery rates. The slow recovery rate and high standard deviation of the recovery data makes samples exposed to RF and no RF indistinguishable. It was initially expected that the RF would induce an electric field that should act to slow the oxide holes drifting to the interface and tunneling out of the oxide, lowering the threshold voltage. The results from previous RF testing suggest that while not under irradiation, the RF acts to increase the threshold voltage. After irradiation, the threshold voltage is expected to recover at a faster rate owing to the RF de-trapping holes in the oxide. Neither an accelerated or slowed rate was observed in the recovery rate of the threshold voltage or in the rate of damage during irradiation. A MOSFET with fewer deep stable oxide traps could be used to show post irradiation threshold voltage recovery in MOSFETs with RF applied to the gate.

One would expect for the threshold voltage to recover to near initial values after irradiation. This process in MOSFETs can take on the order of tens to hundreds of hours [15]. Based on the results of Kim and the results of this work, the RF will decrease the recovery rate of the threshold voltage and even increase the rate of threshold voltage change during irradiation. This can be determined by future research by taking more measurements under different conditions. Methods for performing these measurements are discussed in Chapter 5.

V. Conclusions

5.1 Considerations For Future Testing

While the measurements reported in the document did not provide conclusive results for the hypothesis presented, they should serve as a base for future research. It is clear that, first and foremost, sample selection is important. Ma and Dressendorfer cite examples of MOSFETs that can recover to initial threshold voltage levels or beyond (super recovery/rebound) in a matter of 100 to 1000 hours [15]. It is important to find a MOSFET that exhibits a quick post irradiation threshold voltage recovery. This would allow the researcher to more easily compare results and observe any of the effects that the RF would have on the sample. Another way to increase this anneal rate is to thermally excite the charges within the oxide layer by heating the samples during recovery. Thermal annealing is known to increase the recovery rate and could be of use if samples chosen exhibit slow recovery rates [15]. Samples with numerous deep, stable oxide traps that reside far from the interface are likely to cause these slow recovery rates. Selecting a device with a cleaner oxide (fewer traps) and possibly with a thinner oxide layer or traps that reside closer to the interface should provide this quicker recovery rate. The problem with selecting devices with these characteristics is that knowledge of the recovery rate is will come from experimentation since manufacturers rarely irradiate devices and include those results with factory specification sheets.

Secondly, the experiment itself could be organized and executed more effectively. Some of the equipment selected and measurement methods used could be modified to provide more efficient data measuring procedures. The largest mistake was that of

getting a compliance limit within the 4200 SCS while taking I-V measurements. This could be modified by using a current divider. Two resistors in parallel with one grounded would increase the source to drain resistance, reducing drain to source current at all voltages. This would allow the saturation regions to be plotted after accounting for the added source to drain resistance. Using a current divider is critical for observation of more than just the linear region of the I-V curves and provides further insight into device response to RF and gamma irradiation.

Lastly, many MOSFETs (and electronics in general) are sensitive to electrostatic discharge (ESD). Some electronics have very high sensitivity to ESD. The Fairchild MOSFET devices used in experiments for this document were particularly sensitive to ESD. Several samples quit operating after random time intervals. The only logical reason to explain this abrupt device failure was ESD. This failure is attributed to the method of storage and transport of these devices. The plastic containers in which they were stored likely built up static and discharged, harming the MOSFETs. Also being transported in a vehicle on a dry day likely increased the probability of an ESD. In future projects special static free containers should be used to store and transport all MOSFET devices. Care should also be taken to work on grounded surfaces to greatly reduce any chance of ESD.

5.2 Concluding Remarks

The lessons learned while performing this research have been invaluable to the researcher. The data taken, as stated above, is far from perfect. However, the results have opened the door for future testing. It is this researcher's hope that this data will

form the basis for continued measurements into the area of radiation effects on electronics coupled with RF signals applied to the gate. This area of research will continue to expand the knowledge of susceptibility to electronic warfare and enhance understanding of how devices sustain and survive intentional directed energy attacks in harsh radiation environments.

Appendix A. Definition and References for the dBm Power System

Table 4. References to Common dBm Ranges and Power [26]

dBm	Power	Notes
80	100 kW	*Typical Transmission Power of FM Radio Station with 50 km range*
60	1000 W	*Typical Combined Radiated RF Power of Microwave Oven Elements*
50	100 W	*Typical Thermal Radiation Emitted by a Human Body*
40	10 W	
36	4 W	*Typical Maximum Output power of a Citizens' Band radio Station (27 MHz)*
33	2 W	*Maximum Output from a UMTS/3G (Power Class 1 Mobile Phone)*
30	1000 mW	*Typical RF Leakage From a Microwave Oven*
27	500 mW	*Typical Cellular Telephone Transmission Power and Power Class 2 Mobile Phones*
26	400 mW	
25	316 mW	
24	250 mW	*Maximum Output from Power Class 3 Mobile Phones*
23	200 mW	
22	160 mW	
21	125 mW	*Maximum Output from Power Class 4 Mobile Phones*
20	100 mW	*Bluetooth Class 1 Radio 100m Range, Typical Wireless Router Transmission Power*
15	32 mW	*Typical WiFi Transmission Power in Laptops*
10	10 mW	
6	4 mW	
5	3.2 mW	
4	2.5 mW	*Bluetooth Class 2 Radio 10m Range*
3	2 mW	
2	1.6 mW	
1	1.3 mW	
0	1000 μW	*Bluetooth Standard Class 3 Radio 1m Range*
-1	794 μW	
-3	501 μW	
-5	316 μW	
-10	100 μW	*Typical Maximum Received Signal Power of Wireless Network (-10 to -30 dBm)*
-20	10 μW	
-30	1000 nW	
-40	100 nW	
-50	10 nW	
-60	1000 pW	*The Earth Receives 1 Nanowatt per Square Meter From a Magnitude 3.5 Star*
-70	100 pW	*Typical Range of Received Signal Power From a Wireless Network, 802.11x (-60 to -80 dBm)*
-80	10 pW	
-100	.1 pW	
-111	8 fW	*Thermal Noise Floor For Commercial GPS Single Channel Signal Bandwidth (2 GHz)*
-127.5	178 aW	*Typical Signal Power Received From a GPS Satellite*
-174	4 zW	*Thermal Noise Floor For a 1Hz Bandwidth at Room Temperature (293 K)*
-192.5	56 yW	*Thermal Noise Floor For a 1Hz Bandwidth in Outer Space (4 K)*
-∞	0 W	*Zero Power Not Well Expressed With the dBm Scale*

Table 5. Conversions used in Table 3

Conversions	
1 kW	1000 W
1 W	1000 mW
1 mW	1000 μw
1 μW	1000 nW
1 nW	1000 pW
1 pW	1000 fW
1 fW	1000 aW
1 aW	1000 zW
1 zW	1000 yW

dBm is an abbreviation for the power ratio decibels (dB) of the measured power referenced to one milliwatt (mW). It is used in microwave systems as a convenient measure of absolute power because of its ability to express both very large and very small values in a short form [26]. Equation (14) can be used to describe the relationship between dBm and Power.

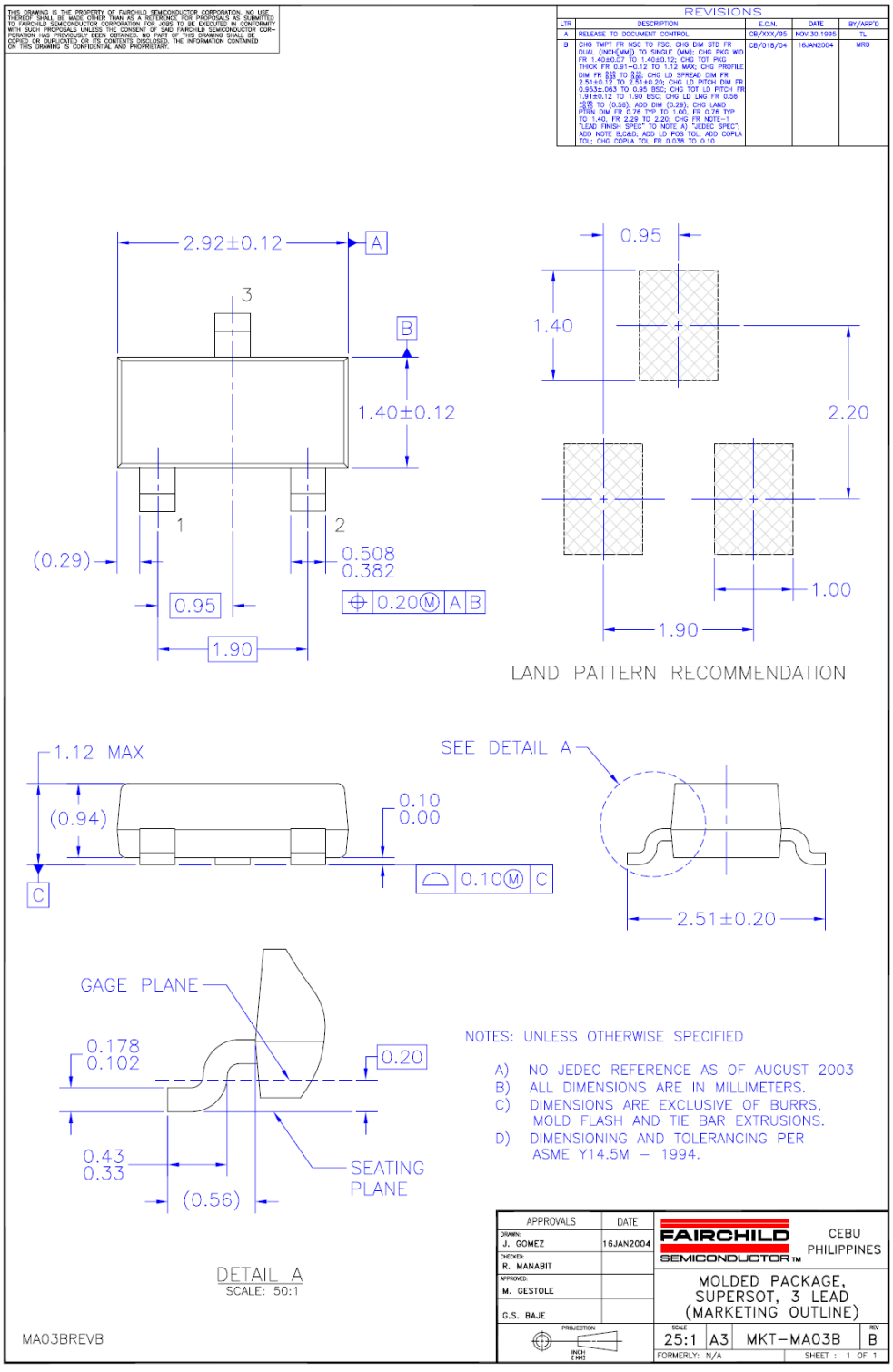
$$x = 10\log_{10}\left(1000P\right) \tag{14}$$

Where x is in dBm and P is in Watts (can be arbitrary). The inverse relationship is shown below in Equation (15).

$$P = \frac{10^{\frac{x}{10}}}{1000} \tag{15}$$

Where Power is in Watts and x is the power ratio in dBm.

Appendix B. Fairchild NDS352AP MOSFET Specifications



FAIRCHILD SEMICONDUCTOR™

February 1997

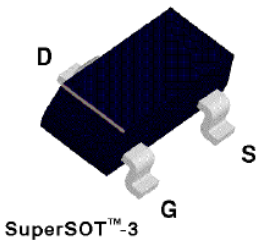
NDS352AP
P-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

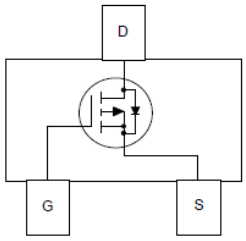
These P -Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management, portable electronics, and other battery powered circuits where fast high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- -0.9 A, -30 V. $R_{DS(ON)}$ = 0.5 Ω @ V_{GS} = -4.5 V
  $R_{DS(ON)}$ = 0.3 Ω @ V_{GS} = -10 V.
- Industry standard outline SOT-23 surface mount package using proprietary SuperSOT™-3 design for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.



SuperSOT™-3



Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS352AP	Units
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage - Continuous		±20	V
I_D	Maximum Drain Current - Continuous	(Note 1a)	±0.9	A
	- Pulsed		±10	
P_D	Maximum Power Dissipation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-1	µA
		T_J =125°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-0.8	-1.7	-2.5	V
		T_J =125°C	-0.5	-1.4	-2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -4.5 V, I_D = -0.9 A		0.45	0.5	Ω
		T_J =125°C		0.65	0.7	
		V_{GS} = -10 V, I_D = -1 A		0.25	0.3	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = -4.5 V, V_{DS} = -5 V	-2			A
g_{FS}	Forward Transconductance	V_{DS} = -5 V, I_D = -0.9 A		1.9		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz		135		pF
C_{oss}	Output Capacitance			88		pF
C_{rss}	Reverse Transfer Capacitance			40		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn - On Delay Time	V_{DD} = -6 V, I_D = -1 A, V_{GS} = -4.5 V, R_{GEN} = 6 Ω		5	10	ns
t_r	Turn - On Rise Time			17	30	ns
$t_{d(off)}$	Turn - Off Delay Time			35	70	ns
t_f	Turn - Off Fall Time			30	60	ns
$t_{d(on)}$	Turn - On Delay Time	V_{DD} = -10 V, I_D = -1 A, V_{GS} = -10 V, R_{GEN} = 50 Ω		8	15	ns
t_r	Turn - On Rise Time			16	30	ns
$t_{d(off)}$	Turn - Off Delay Time			35	90	ns
t_f	Turn - Off Fall Time			30	90	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -0.9 A, V_{GS} = -4.5 V		2	3	nC
Q_{gs}	Gate-Source Charge			0.5		nC
Q_{gd}	Gate-Drain Charge			1		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Source Current				-0.42	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				-10	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.42 (Note 2)		-0.8	-1.2	V

Notes:

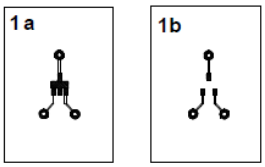
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 250°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

b. 270°C/W when mounted on a 0.001 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

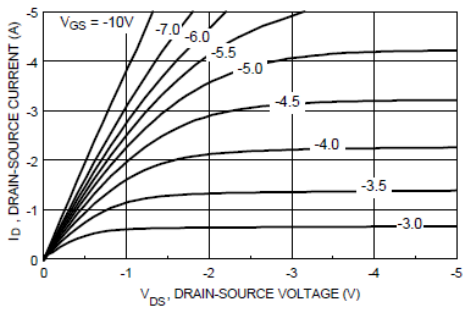


Figure 1. On-Region Characteristics.

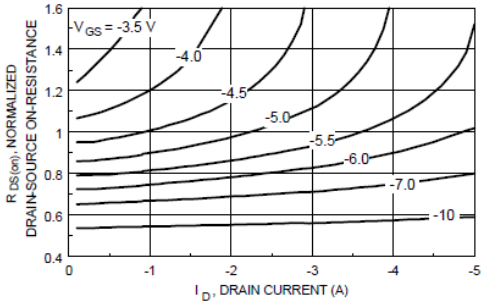


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

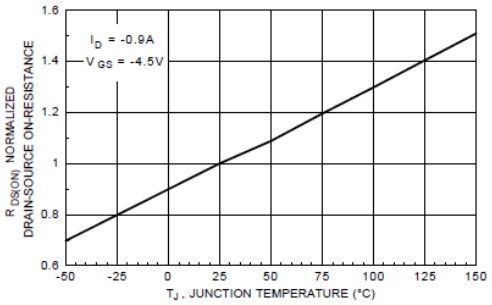


Figure 3. On-Resistance Variation with Temperature.

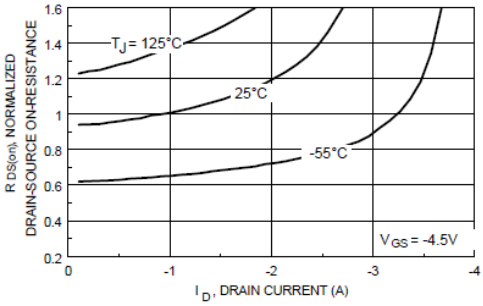


Figure 4. On-Resistance Variation with Drain Current and Temperature.

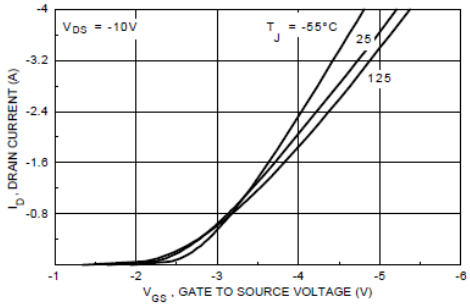


Figure 5. Transfer Characteristics.

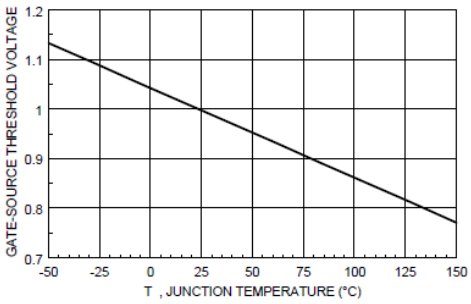


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

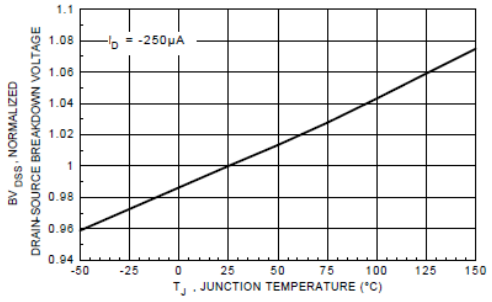


Figure 7. Breakdown Voltage Variation with Temperature.

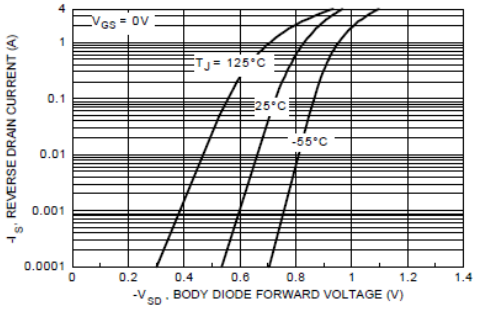


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature.

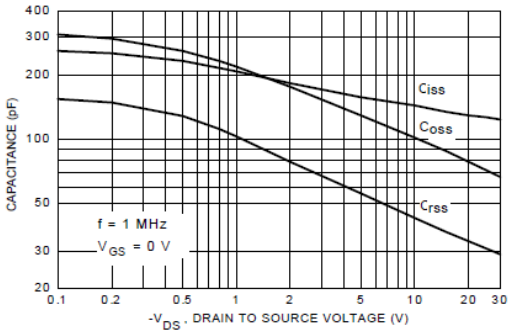


Figure 9. Capacitance Characteristics.

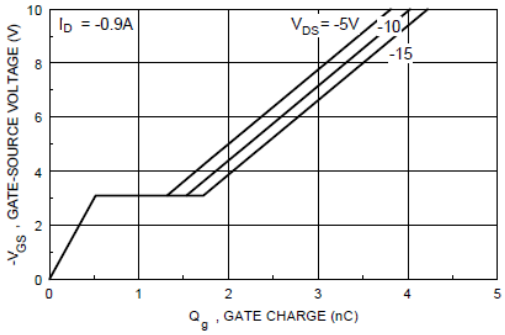


Figure 10. Gate Charge Characteristics.

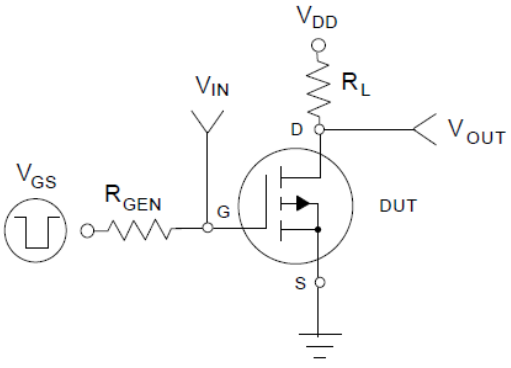


Figure 11. Switching Test Circuit.

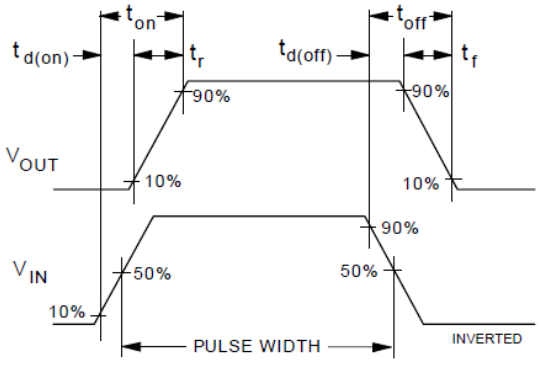


Figure 12. Switching Waveforms.

Typical Electrical Characteristics (continued)

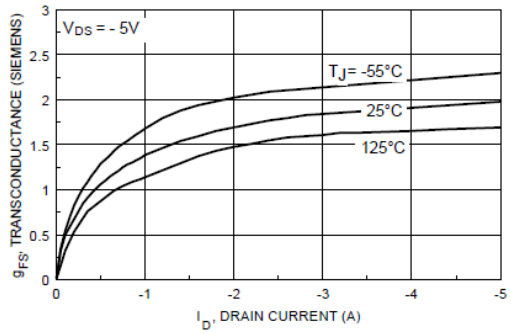


Figure 13. Transconductance Variation with Drain Current and Temperature.

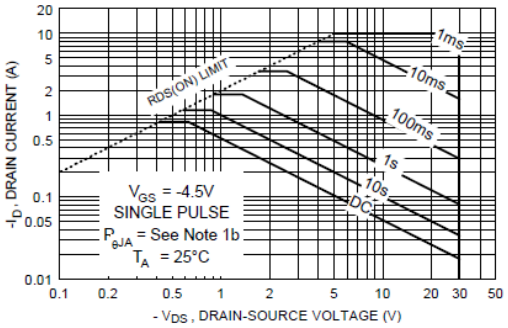
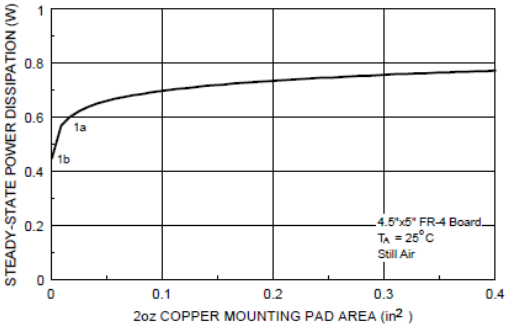


Figure 14. Maximum Safe Operating Area.



Figue 15. SuperSOT™ - 3 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

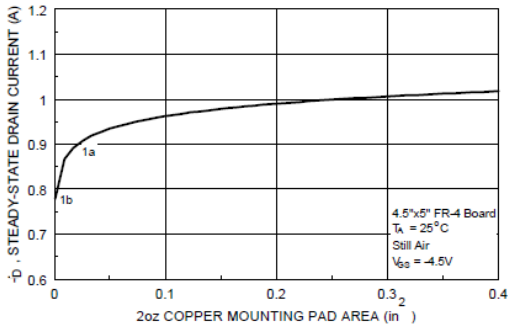


Figure 16. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

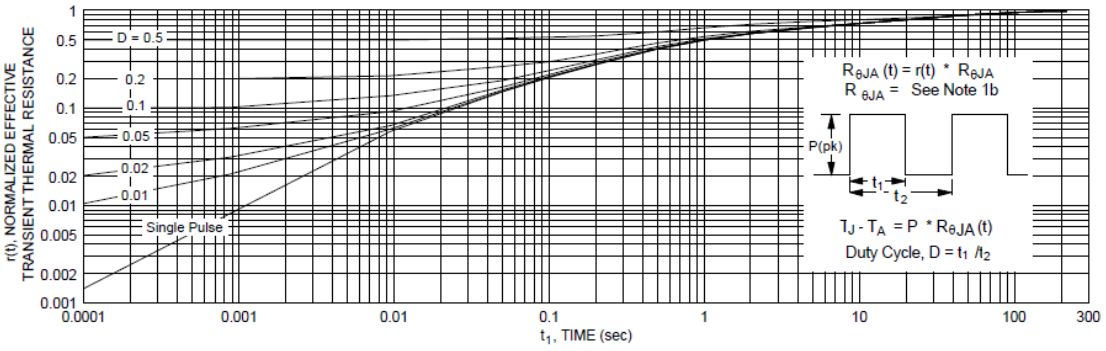
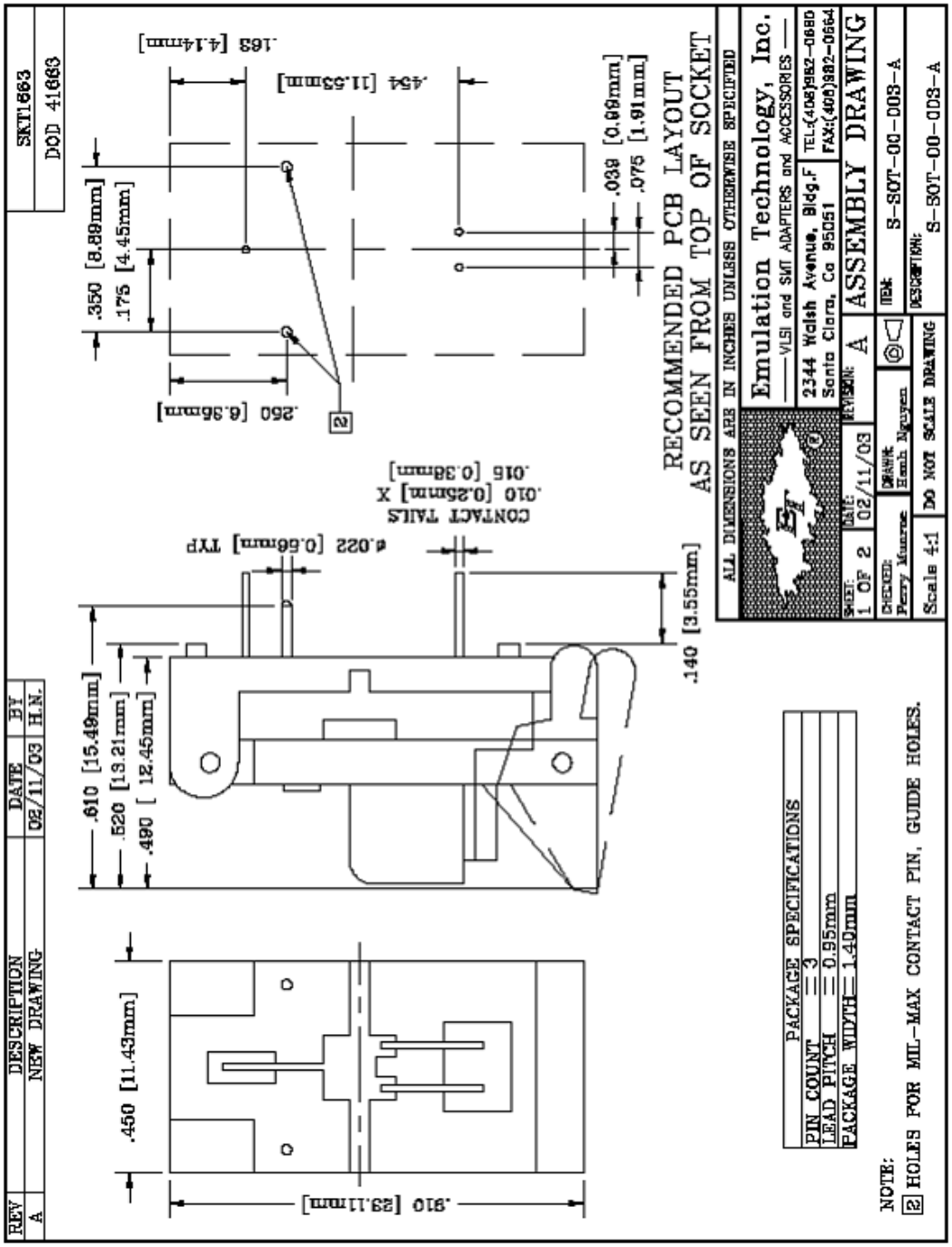


Figure 17. Transient Thermal Response Curve.

Note : Characterization performed using the conditions described in note 1b. Transient thermal response will change depending on the circuit board design.

NDS352Ap Rev.C

Appendix C. Emulation Technology SOT23-3 Cradle Specifications



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14. ABSTRACT

The purpose of this research was to investigate the combined effects of continuous gigahertz radio frequency signals and gamma irradiation on the threshold voltage of metal oxide semiconductor field effect transistors. The Fairchild NDS352AP, a commonly used commercial device, was irradiated by a cobalt-60 source under a +5 V bias with and without a radio frequency signal applied to the gate. The threshold voltage was measured during and after irradiation. During irradiation all devices exhibited an expected negative threshold voltage shift. The application of radio frequency to the gate resulted in a 7.2% increase in the rate of change of the threshold voltage during irradiation. When RF was applied after irradiation it produced no observable change when compared to the results of samples exposed to gamma radiation alone. Few conclusions can be drawn about the effects of radio frequency on post irradiation samples owing to the long recovery time of the samples. Before irradiation the radio frequency demonstrated a 5.95% increase drain current for a given drain to source voltage during I-V measurements. The threshold voltage also increased by 1.57%. The power of the radio frequency signal was adjusted from 1 to 14 dBm with no measurable effect.

15. SUBJECT TERMS

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